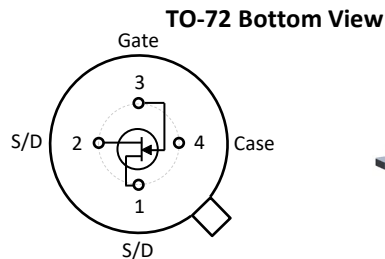


2N4117/A, 2N4118/A, 2N4119/A N-Channel JFET JAN Equivalent Parts

Features

- InterFET [N0001H Geometry](#)
- Low gate leakage: 120fA typical @20V
- Low Ciss: 1.8pF typical
- Typical BV_{GSS}: -60V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- Edge case SPICE modeling: [InterFET SPICE](#)



Industry Standard Crosses

- 2N4117, 2N4118, 2N4119, VCR7N

Built to MIL-PRF-19500

InterFET Similar Parts

- SMP4117-8-9, PNVCR7N

(Source and Drain pins are interchangeable)

InterFET Dual Parts

- IFNU421-2-3-4-5-6

Applications

- General: Buffers; Signal mixers; Femtoampere diodes
- Military/Aero: Radar; Communications; Satellites
- Medical: Imaging systems; Monitors; Ultrasound

Description

The -50V InterFET 2N4117/A, 2N4118/A, and 2N4119/A JFET's are targeted for ultra high input impedance applications. Gate leakages are typically 120fA at room temperatures. Proprietary InterFET processes yield exceptionally high radiation tolerance. Parts can be connected for femtoampere diode applications.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N4117JANequiv, 2N4118JANequiv 2N4119JANequiv	JAN Equivalent 	TO-72	Bulk
2N4117AJANequiv, 2N4118AJANequiv 2N4119AJANequiv	JAN Equivalent	TO-72	Bulk
2N4117JANTXequiv, 2N4118JANTXequiv 2N4119JANTXequiv	JANTX Equivalent	TO-72	Bulk
2N4117AJANTXequiv, 2N4118AJANTXequiv 2N4119AJANTXequiv	JANTX Equivalent	TO-72	Bulk
2N4117JANTXVequiv, 2N4118JANTXVequiv 2N4119JANTXVequiv	JANTXV Equivalent	TO-72	Bulk
2N4117AJANTXVequiv, 2N4118AJANTXVequiv 2N4119AJANTXVequiv	JANTXV Equivalent	TO-72	Bulk
2N4117JANSequiv, 2N4118JANSequiv 2N4119JANSequiv	JANS Equivalent	TO-72	Bulk
2N4117AJANSequiv, 2N4118AJANSequiv 2N4119AJANSequiv	JANS Equivalent	TO-72	Bulk



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	TO-72	SOT-23	TO-92	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-20	-20	-20	V
I_{FG} Continuous Forward Gate Current	50	50	50	mA
P_{D} Continuous Device Power Dissipation ¹	500	350	500	mW
P Power Derating ¹	3.3	2.8	4	mW/ $^\circ\text{C}$
T_{J} Operating Junction Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

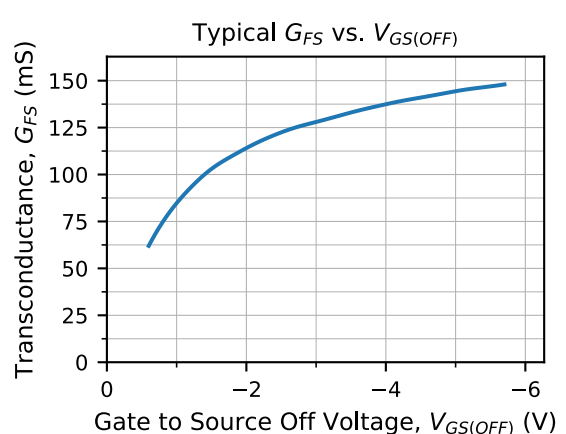
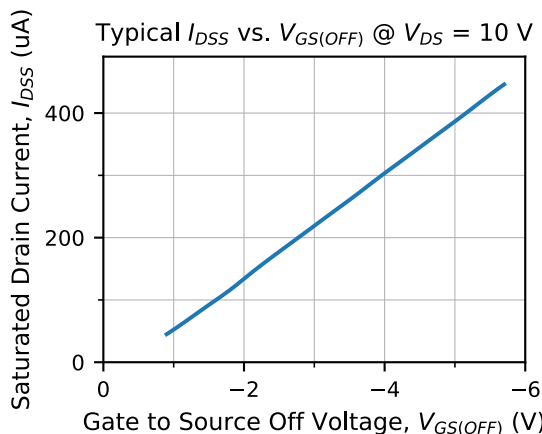
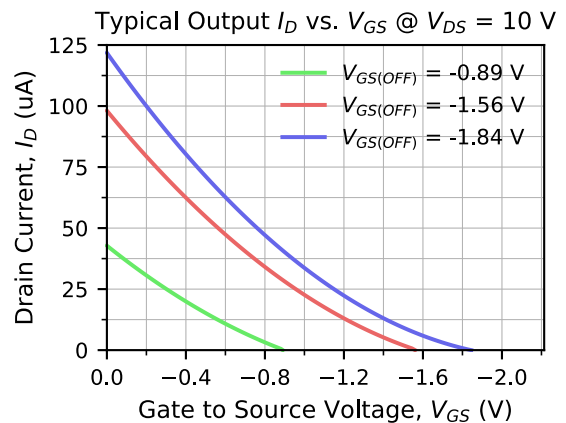
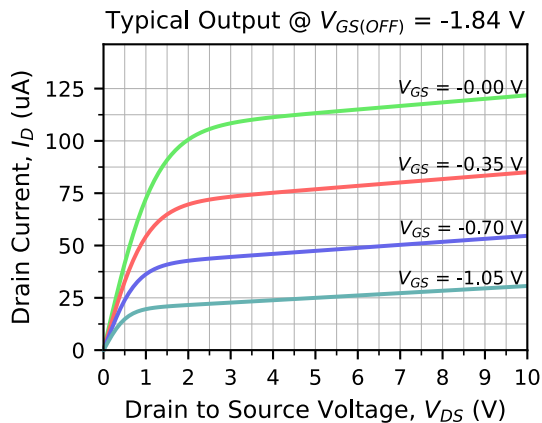
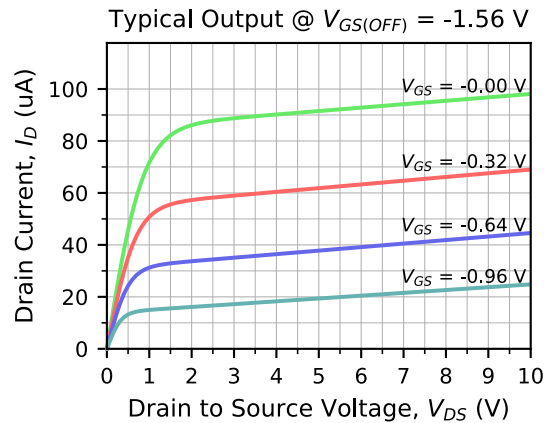
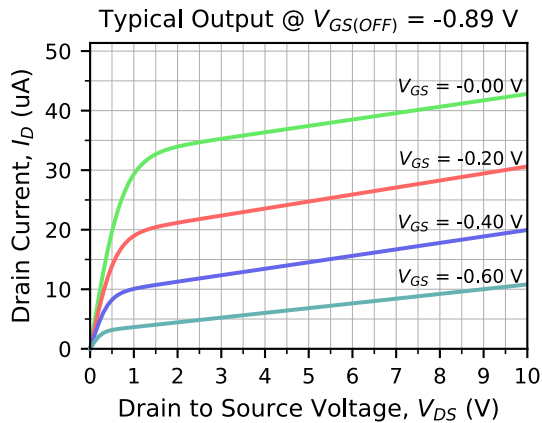
Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified, Highlighted values = A variant)

Parameters	Conditions	2N4117/A		2N4118/A		2N4119/A		Unit
		Min	Max	Min	Max	Min	Max	
$V_{(\text{BR})\text{GSS}}$ Gate to Source Breakdown Voltage	$I_{\text{G}} = -1\mu\text{A}, V_{\text{DS}} = 0\text{V}$	-40		-40		-40		V
I_{GSS} Gate to Source Reverse Current	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$		-10		-10		-10	pA
			-1		-1		-1	pA
$V_{\text{GS}(\text{OFF})}$ Gate to Source Cutoff Voltage	$V_{\text{DS}} = 10\text{V}, I_{\text{D}} = 1\text{nA}$	-0.6	-1.8	-1	-3	-2	-6	V
I_{DSS} Drain to Source Saturation Current	$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 0\text{V}$ (Pulsed)	0.03	0.09	0.08	0.24	0.2	0.6	mA
		0.015	0.09	0.08	0.24	0.2	0.6	mA

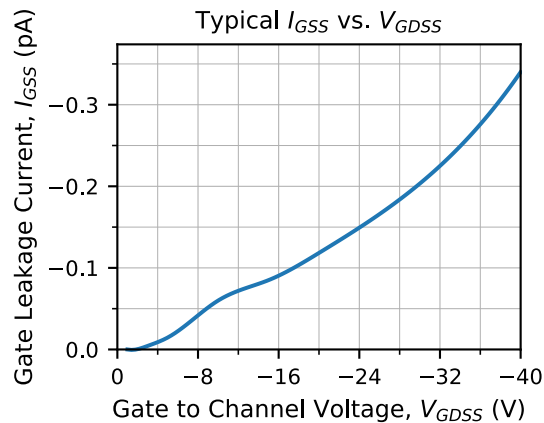
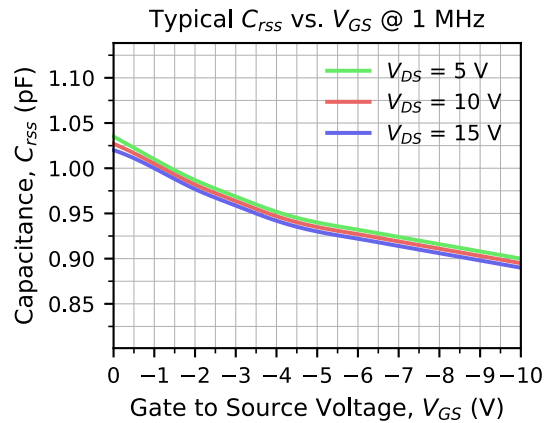
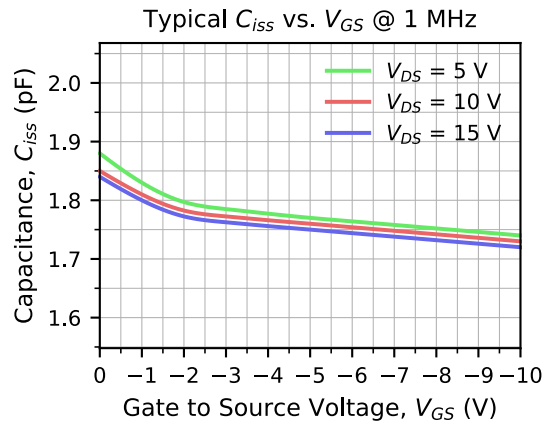
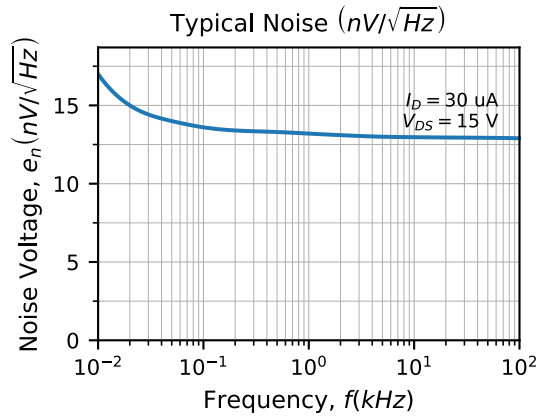
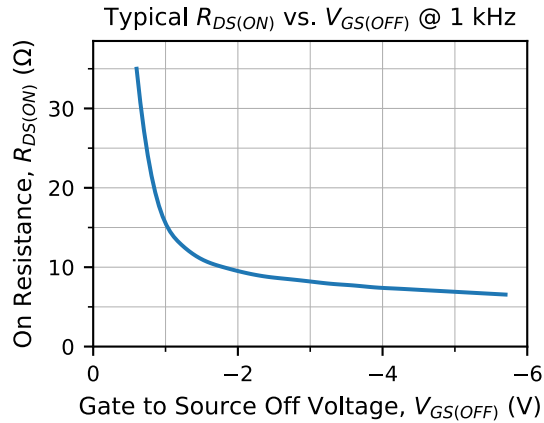
Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N4117/A		2N4118/A		2N4119/A		Unit
		Min	Max	Min	Max	Min	Max	
G_{FS} Forward Transconductance	$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{kHz}$	70	210	80	250	100	330	μS
G_{OS} Output Conductance	$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{kHz}$		3		5		10	μS
C_{iss} Input Capacitance	$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$		3		3		3	pF
C_{rss} Reverse Transfer Capacitance	$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$		1.5		1.5		1.5	pF

Typical 2N4117, 2N4118, 2N4119 Characteristics

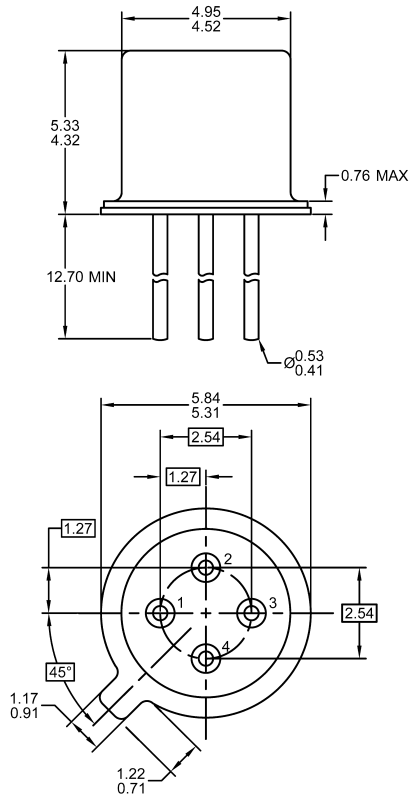


Typical 2N4117, 2N4118, 2N4119 Characteristics (Continued)



TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.



Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit

www.InterFET.com/environmental/.

Legal Notice

InterFET Corporation reserves the right to make corrections, enhancements, improvements, modifications, and other changes to its semiconductor products without further notice to this document and any product described herein. InterFET does not assume any liability arising out of the application or use of this document or any product described herein. Unless InterFET has explicitly designated an individual product as meeting the requirements of a particular industry standard, InterFET is not responsible for any failure to meet such industry standard requirements.

InterFET Corporation assumes no liability for a customers product design or applications. Corporate designers and others who are developing systems that incorporate InterFET products understand and agree that they remain responsible for using their independent analysis, evaluation and judgment in designing their applications. Corporate designers and others have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications with all applicable regulations, laws and other applicable requirements.

InterFET Corporation resources are provided "as is" with potential faults. InterFET disclaims all other warranties or representations, express or implied, regarding resources or use thereof, including but not limited to accuracy or completeness, title, any widespread failure warranty and any implied warranties of merchantability, fitness for a particular purpose, and non-infringement of any third party intellectual property rights. InterFET shall not be liable for and shall not defend or indemnify designer against any claim, including but not limited to any infringement claim that relates to or is based on any combination of products even if described in InterFET resources or otherwise. In no event shall InterFET be liable for any actual, direct, special, collateral, indirect, punitive, incidental, consequential or exemplary damages in connection with or arising out of InterFET resources or use thereof, and regardless of whether InterFET has been advised of the possibility of such damages.