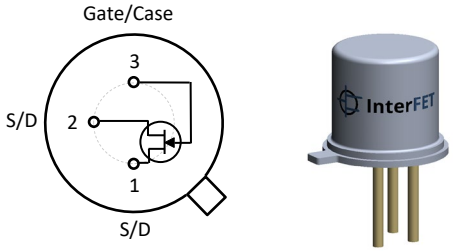
2N4391, 2N4392, 2N4393 N-Channel JFET
Jan equivalent parts

Features

- InterFET N0132S Geometry
- Low noise: 1.0 nV/√Hz typical
- High gain: 22mS typical
- Low gate leakage: 750fA typical @20V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- Edge case SPICE modeling: InterFET SPICE

TO-18 Bottom View



InterFET Similar Parts

- 2N3970-1-2, 2N4091-2-3, 2N4856-7-8A, 2N4859-60-61A
- IFN113
- J111-2-3

Built to MIL-PRF-19500

(Source and Drain pins are interchangeable)

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone preamplifiers
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The -40V InterFET 2N4391, 2N4392 and 2N4393 are targeted for switch, chopper and commutator designs. Gate leakages are typically less than 50pA at room temperatures. The 2N4393 has a cutoff voltage of less than 3.0V ideal for low-level power supplies. The TO-18 package is hermetically sealed and suitable for military applications.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N4391JANequiv, 2N4392JANequiv 2N4393JANequiv	JAN equivalent	TO-18	Bulk
2N4391JANTXequiv, 2N4392JANTXequiv 2N4393JANTXequiv	JANTX equivalent	TO-18	Bulk
2N4391JANTXVequiv, 2N4392JANTXVequiv 2N4393JANTXVequiv	JANTXV equivalent	TO-18	Bulk
2N4391JANSequiv, 2N4392JANSequiv 2N4393JANSequiv	JANS equivalent	TO-18	Bulk

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		TO-18	SOT-23	TO-92	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	-20	-20	V
I_{FG}	Continuous Forward Gate Current	50	50	50	mA
P_D	Continuous Device Power Dissipation[1]	500	350	500	mW
P	Power Derating[1]	3.3	2.8	4	mW/°C
T_J	Operating Junction Temperature	-65 to 175	-55 to 150	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 175	-55 to 150	-55 to 150	°C

[1] Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

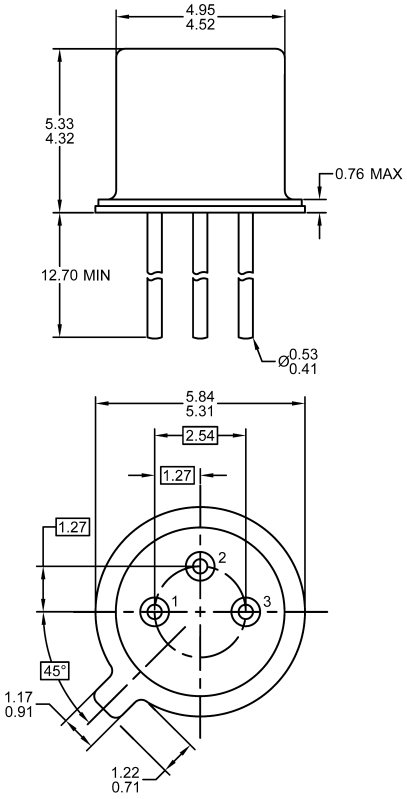
Parameters		Conditions	2N4391		2N4392		2N4393		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-40		-40		-40		V
I_{GSS}	Gate to Source Reverse Current	V_{DS} = -20V, V_{GS} = 0V, T_A = 25°C		-100		-100		-100	pA
		V_{DS} = -20V, V_{GS} = 0V, T_A = 150°C		-200		-200		-200	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA	-4	-10	-2	-5	-0.5	-3	V
$V_{GS(F)}$	Gate to Source Forward Voltage	V_{DS} = 0V, I_G = 1mA		1		1		1	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 20V (Pulsed)	50	150	25	75	5	30	mA
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = 20V, V_{GS} = -5V, T_A = 25°C						100	pA
		V_{DS} = 20V, V_{GS} = -5V, T_A = 150°C						200	nA
		V_{DS} = 20V, V_{GS} = -7V, T_A = 25°C				100			pA
		V_{DS} = 20V, V_{GS} = -7V, T_A = 150°C				200			nA
		V_{DS} = 20V, V_{GS} = -12V, T_A = 25°C		100					pA
		V_{DS} = 20V, V_{GS} = -12V, T_A = 150°C		200					nA
$V_{DS(ON)}$	Drain to Source ON Voltage	V_{GS} = 0V, I_D = 3mA						0.4	V
		V_{GS} = 0V, I_D = 6mA				0.4			
		V_{GS} = 0V, I_D = 12mA		0.4					
$R_{DS(ON)}$	Static Drain to Source ON Resistance	V_{GS} = 0V, I_D = 1mA		30		60		100	Ω

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	2N4391		2N4392		2N4393		Unit
			Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{GS} = 0V, I_D = 0A, f = 1kHz		30		60		100	Ω
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		14		14		14	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 0V, V_{GS} = -5V, f = 1MHz						3.5	pF
		V_{DS} = 0V, V_{GS} = -7V, f = 1MHz				3.5			
		V_{DS} = 0V, V_{GS} = -12V, f = 1MHz		3.5					
t_d	Turn-On Delay Time	V_{DD} = 10V, $V_{GS(ON)}$ = 0V		15		15		15	ns
t_r	Rise Time	V_{DD} = 10V, $V_{GS(ON)}$ = 0V		5		5		5	ns
$t_{D(OFF)}$	Turn-Off Delay Time	V_{DD} = 10V,$V_{GS(ON)}$ = 0V		20		35		50	ns
t_f	Fall Time	V_{DD} = 10V,$V_{GS(ON)}$ = 0V		15		20		30	ns

TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

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