

2N4856/A, 2N4857/A, 2N4858/A N-Channel JFET JAN Equivalent Parts

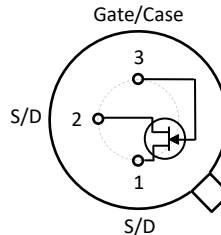
Features

- InterFET [N0132S Geometry](#)
- Low noise: 1.0 nV/√Hz typical
- High gain: 22mS typical
- Low gate leakage: 750fA typical @20
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- Edge case SPICE modeling: [InterFET SPICE](#)

InterFET Similar Parts

- 2N3970, 2N4391
- IFN113

TO-18 Bottom View



Built to MIL-PRF-19500

(Source and Drain pins are interchangeable)

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The -40V InterFET 2N4856/A, 2N4857/A, and 2N4858/A JFET's are targeted for very low noise switching applications for mid to high frequency designs. Gate leakages are typically 50pA at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications.

Ordering Information

Part Number	Description	Case	Packaging
2N4856JANequiv; 2N4857JANequiv 2N4858JANequiv;	JAN equivalent	TO-18	Bulk
2N4856AJANequiv; 2N4857AJANequiv 2N4858AJANequiv;	JAN equivalent	TO-18	Bulk
2N4856JANTXequiv; 2N4857JANTXequiv 2N4858JANTXequiv;	JANTX equivalent	TO-18	Bulk
2N4856AJANTXequiv; 2N4857AJANTXequiv 2N4858AJANTXequiv;	JANTX equivalent	TO-18	Bulk
2N4856JANTXVequiv; 2N4857JANTXVequiv 2N4858JANTXVequiv;	JANTXV equivalent	TO-18	Bulk
2N4856AJANTXVequiv; 2N4857AJANTXVequiv 2N4858AJANTXVequiv;	JANTXV equivalent	TO-18	Bulk
2N4856JANSequiv; 2N4857JANSequiv 2N4858JANSequiv;	JANS equivalent	TO-18	Bulk
2N4856AJANSequiv; 2N4857AJANSequiv 2N4858AJANSequiv;	JANS equivalent	TO-18	Bulk



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	TO-72	SOT-23	TO-92	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-20	-20	-20	V
I_{FG} Continuous Forward Gate Current	50	50	50	mA
P_D Continuous Device Power Dissipation ¹	500	350	500	mW
P Power Derating ¹	3.3	2.8	4	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$

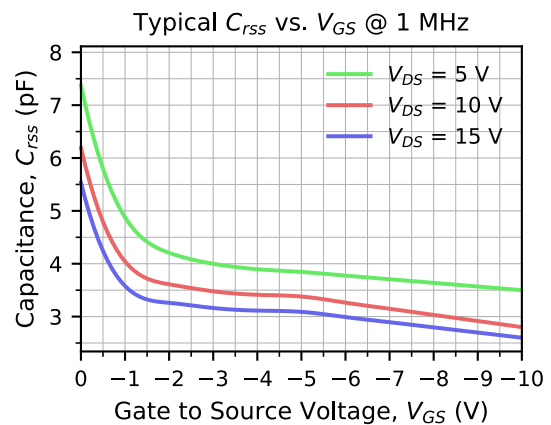
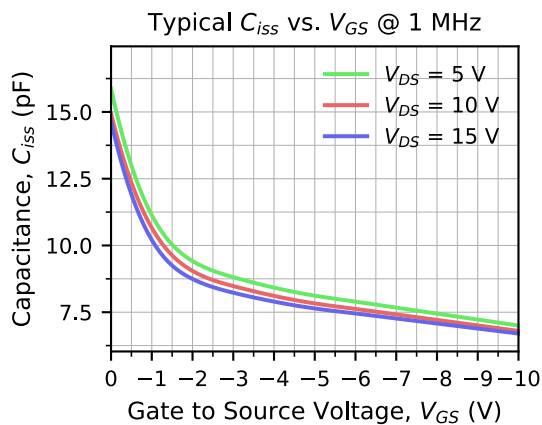
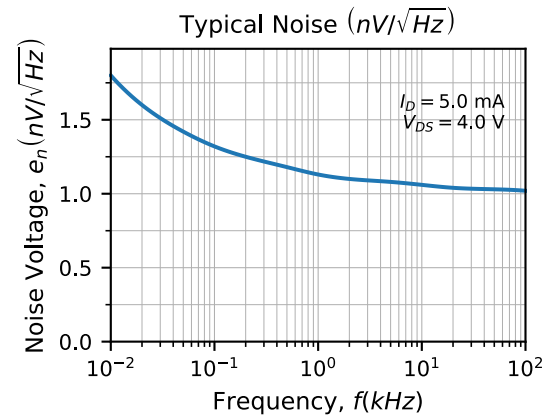
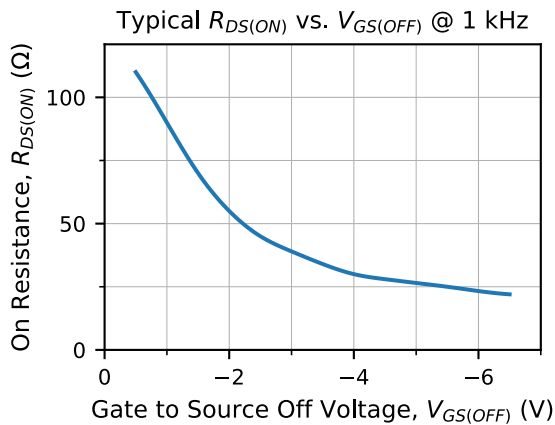
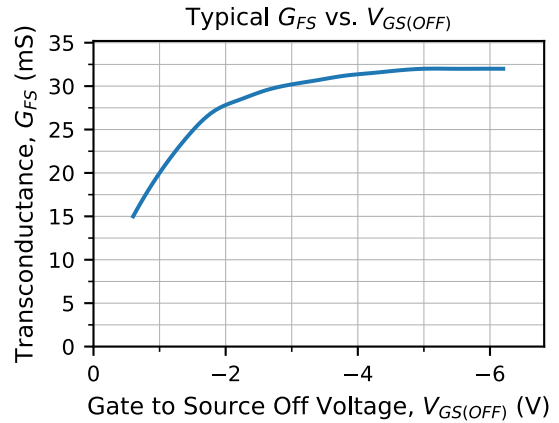
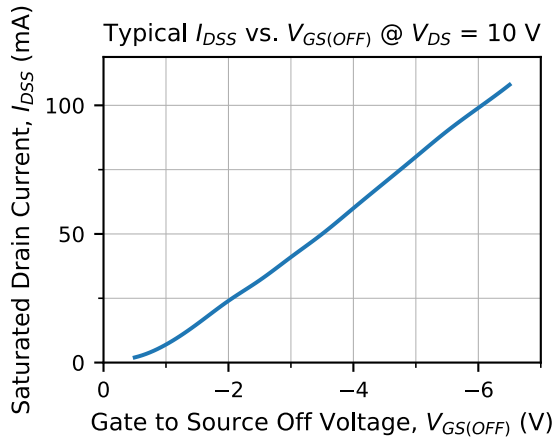
¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

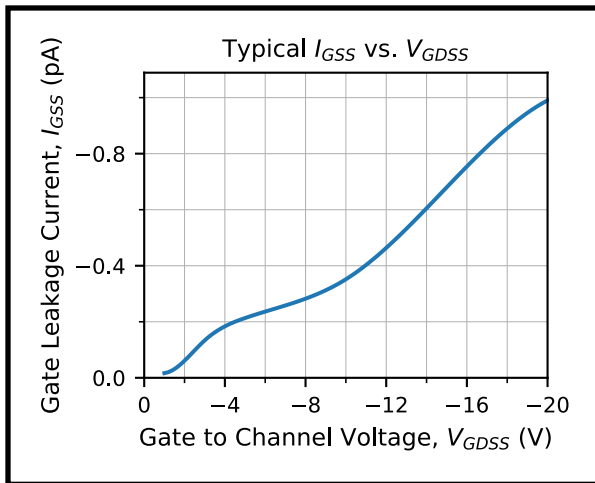
Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified, Highlighted values = A variant)

Parameters	Conditions	2N4856/A		2N4857/A		2N4858/A		Unit
		Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0\text{V}$	-40		-40		-40		V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -20\text{V}, V_{DS} = 0\text{V}, T_A = 25^\circ\text{C}$		-250		-200		-200	pA
	$V_{GS} = -20\text{V}, V_{DS} = 0\text{V}, T_A = 150^\circ\text{C}$		-500		-500		-500	nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 15\text{V}, I_D = 0.5\text{nA}$	-4	-10	-2	-6	-0.8	-4	V
I_{DSS} Drain to Source Saturation Current	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}$ (Pulsed)	50		20	100	8	80	mA
$I_{D(OFF)}$ Drain Cutoff Current	$V_{DS} = 15\text{V}, V_{GS} = -10\text{V}, T_A = 25^\circ\text{C}$		250		250		250	pA
	$V_{DS} = 15\text{V}, V_{GS} = -10\text{V}, T_A = 150^\circ\text{C}$		500		500		500	nA
$V_{DS(ON)}$ Drain to Source ON Voltage	$V_{GS} = 0\text{V}, I_D = ()$		0.75 (20)		0.5 (10)		0.5 (5)	V mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified, Highlighted values = A variant)

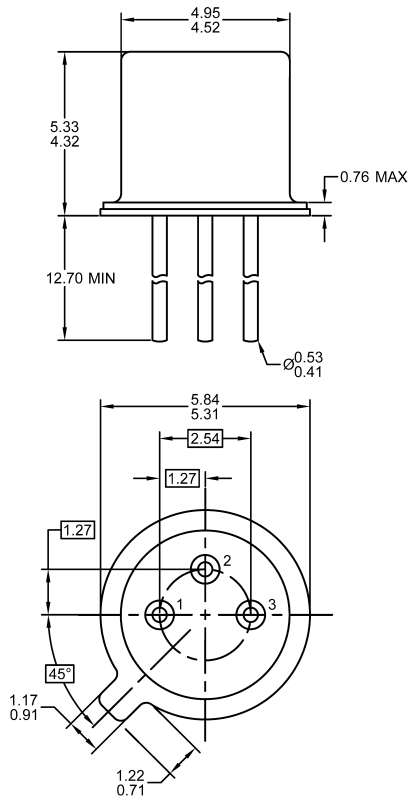
Parameters	Conditions	2N4856/A		2N4857/A		2N4858/A		Unit
		Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$ Drain to Source ON Resistance	$V_{GS} = 0\text{V}, I_D = 0\text{A},$ $f = 1\text{kHz}$		25		40		60	Ω
C_{iss} Input Capacitance	$V_{DS} = 0\text{V}, V_{GS} = -10\text{V},$ $f = 1\text{MHz}$		18		18		18	pF
			10		10		10	
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 0\text{V}, V_{GS} = -10\text{V},$ $f = 1\text{MHz}$		8		8		8	pF
			4		3.5		3.5	
$t_{d(on)}$ Turn-On Delay Time	$V_{DD} = 10\text{V}, V_{GS(ON)} = 0\text{V}$ $I_{D(ON)} = (), V_{GS(OFF)} = []$		6		6		10	ns
			5		6		8	
			(20)		(10)		(5)	(mA)
			[-10]		[-6]		[-4]	[V]
t_r Rise Time	$V_{DD} = 10\text{V}, V_{GS(ON)} = 0\text{V}$ $I_{D(ON)} = (), V_{GS(OFF)} = []$		3		4		10	ns
			3		4		8	
			(20)		(10)		(5)	(mA)
			[-10]		[-6]		[-4]	[V]
$t_{d(off)}$ Turn-Off Delay Time	$V_{DD} = 10\text{V}, V_{GS(ON)} = 0\text{V}$ $I_{D(ON)} = (), V_{GS(OFF)} = []$		25		50		100	ns
			25		40		80	
			(20)		(10)		(5)	(mA)
			[-10]		[-6]		[-4]	[V]





TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.



Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit

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