







2N5457 N-Channel JFET

Features

- InterFET N0032H Geometry
- Low Noise: 7 nV/VHz Typical
- Low Ciss: 6pF Typical
- · RoHS Compliant
- SMT, TH, and Bare Die Package options.

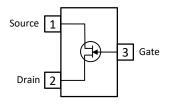
Applications

- · Audio Amplifiers
- · General Purpose Amplifiers
- Switches

Description

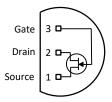
The -25V InterFET 2N5457 JFET is targeted for low noise switching and audio amplifier applications. Gate leakages are typically less than 10pA at room temperatures.

SOT23 Top View





TO-92 Bottom View





Product Summary

	Parameters	2N5457 Min	Unit	
BV _{GSS}	Gate to Source Breakdown Voltage	25	V	
I _{DSS}	Drain to Source Saturation Current	1	mA	
V _{GS(off)}	Gate to Source Cutoff Voltage	-0.5	V	
GFS	Forward Transconductance	1000	μS	

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N5457	Through-Hole	TO-92	Bulk
SMP5457	Surface Mount	SOT23	Bulk
	7" Tape and Reel: Max 3,000 Pieces		Minimum 1,000 Pieces
SMP5457TR	13" Tape and Reel: Max 9,000 Pieces	SOT23	Tape and Reel
2N5457COT	Chip Orientated Tray (COT Waffle Pack)	СОТ	400/Waffle Pack
2N5457CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.









Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

	Parameters	Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	25	V
I _{FG}	Continuous Forward Gate Current	10	mA
PD	Continuous Device Power Dissipation	310	mW
Р	Power Derating	2.82	mW/°C
Τı	Operating Junction Temperature	-65 to 135	°C
T _{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

			2N5457		
	Parameters	Conditions	Min	Max	Unit
V _{(BR)GSS}	Gate to Source Breakdown Voltage	V _{DS} = 0V, I _G = 10μA	-25		V
I _{GSS}	Gate to Source Reverse Current	$V_{GS} = 15V$, $V_{DS} = 0V$, $T_A = 25$ °C $V_{GS} = 15V$, $V_{DS} = 0V$, $T_A = 100$ °C		1 200	nA
V _{GS(OFF)}	Gate to Source Cutoff Voltage	V _{DS} = 15V, I _D = 10nA	-0.5	-6.0	V
I _{DSS}	Drain to Source Saturation Current	$V_{GS} = 0V$, $V_{DS} = 15V$ (Pulsed)	1	5	mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

			2N5457		
	Parameters	Conditions	Min	Max	Unit
G _{FS}	Forward Transconductance	V _{DS} = 15V, V _{GS} = 0V, f = 1kHz	1000	5000	μS
Gos	Output Conductance	V _{DS} = 15V, V _{GS} = 0V, f = 1kHz		50	μS
Ciss	Input Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz		7	pF
Crss	Reverse Transfer Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz		3	pF



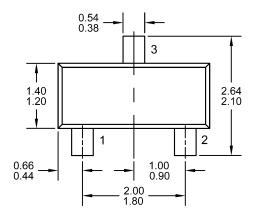


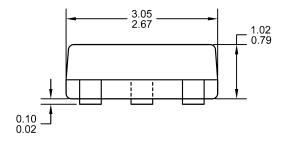


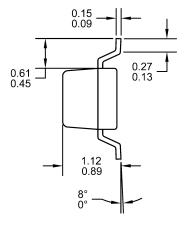


SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

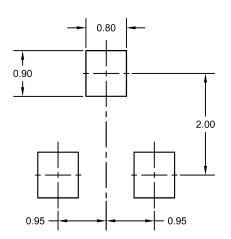






- 1. All linear dimensions are in millimeters.
- 2. Package weight approximately 0.12 grams
- 3. Molded plastic case UL 94V-0 rated
- For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
- Bulk product is shipped in standard ESD shipping material
- 6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



- 1. All linear dimensions are in millimeters.
- 2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.



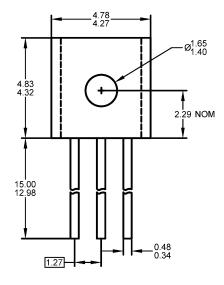


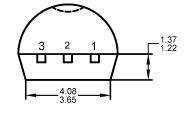


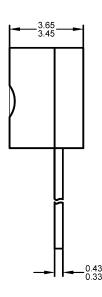


TO-92 Mechanical and Layout Data

Package Outline Data

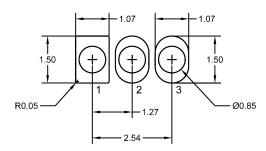






- 1. All linear dimensions are in millimeters.
- 2. Package weight approximately 0.19 grams
- 3. Molded plastic case UL 94V-0 rated
- Bulk product is shipped in standard ESD shipping material
- 5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



- 1. All linear dimensions are in millimeters.
- The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.