

IF150A, IF150B, IF150C N-Channel JFET

Features

- InterFET [N0014LX Geometry](#)
- Low gate leakage: 100fA typical @5V
- Low Ciss: 3pF typical
- Typical noise: 3.0 nV/√Hz
- Typical gain: 7mS
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: [InterFET SPICE](#)

Industry Standard Crosses

- IF142, BF512, SST4416, SST4416A, MMBF4416
- MMBF4416A, MMBF5485, SSTJ211

InterFET Similar Parts

- IFBF512, 2N4416, J304, 2N4303, 2N5485, J211,
- IF140, IF140A, SMP4416, SMPJ304, SMP4303, SMP5485, SMPJ211

InterFET Dual Parts

- IFN5911, IFN5912

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone preamplifiers
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

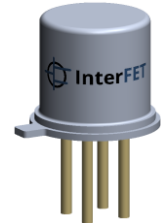
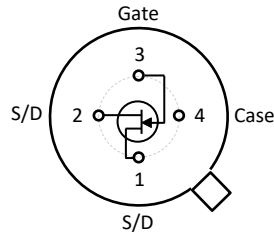
Description

The -10V InterFET IF150A, IF150B, and IF150C are the lowest leakage mid-gain JFET products on the market. Targeted for low noise higher frequencies designs these JFETs are ideal for medical and military applications. Gate leakages are typically 100fA at room temperatures. Higher gain binned version of IF140.

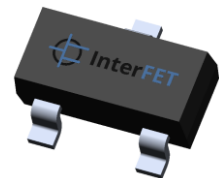
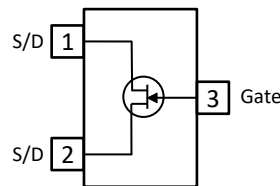
Ordering Information

Part Number	Description	Case	Packaging
IF150AT72; IF150BT72; IF150CT72	Through-Hole	TO-72	Bulk
IF150AST3; IF150BST3; IF150CST3	Surface Mount	SOT23	Bulk
IF150AST3TR; IF150BST3TR; IF150CST3TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
IF150ACOT; IF150BCOT; IF150CCOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IF150ACFT; IF150BCFT; IF150CCFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

TO-72 Bottom View



SOT23 Top View



NOTE: S/D pins are interchangeable Source Drain connections



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	TO-72	SOT-23	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-10	-10	V
I_{FG} Continuous Forward Gate Current	50	50	mA
P_D Continuous Device Power Dissipation ¹	500	350	mW
P Power Derating ¹	3.3	2.8	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-65 to 175	-55 to 150	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 175	-55 to 150	$^\circ\text{C}$

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

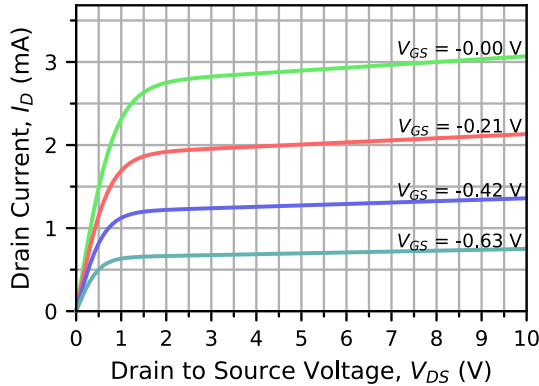
Parameters	Conditions	IF150A		IF150B		IF150C		Unit
		Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu A$	-10		-10		-10		V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -5V, V_{DS} = 0V, T_A = 25^\circ\text{C}$ $V_{GS} = -5V, V_{DS} = 0V, T_A = 150^\circ\text{C}$		-5 -200		-5 -200		-5 -200	pA pA
$V_{GS(F)}$ Gate to Source Forward Voltage	$V_{DS} = 0V, I_G = 1mA$		1		1		1	V
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 8V, I_D = 5nA$	-0.8	-2.0	-1.8	-3.2	-3.0	-6.0	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 8V$ (Pulsed)	0.5	3.5	3.0	10	8	22	mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

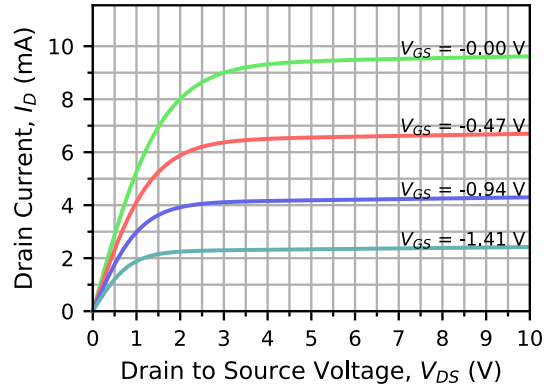
Parameters	Conditions	IF150A		IF150B		IF150C		Unit
		Min	Max	Min	Max	Min	Max	
G_{FS} Forward Transconductance	$V_{DS} = 8V, V_{GS} = 0V, f = 1kHz$	1.0		3.0		5.0		mS
G_{OS} Output Conductance	$V_{DS} = 8V, V_{GS} = 0V, f = 1kHz$		0.05		0.05		0.05	mS
C_{iss} Input Capacitance	$V_{DS} = 8V, V_{GS} = 0V, f = 1MHz$		3		3		3	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 8V, V_{GS} = 0V, f = 1MHz$		1.2		1.2		1.2	pF
e_n Equivalent Circuit Input Noise Voltage	$V_{DS} = 8V, V_{GS} = 0V, f = 10Hz$	3 (typ)		3 (typ)		3 (typ)		nV/ $\sqrt{\text{Hz}}$

Typical IF150 Characteristics

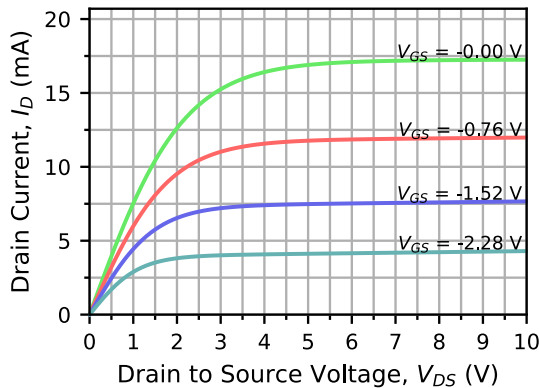
Typical Output @ $V_{GS(OFF)} = -1.53 \text{ V}$



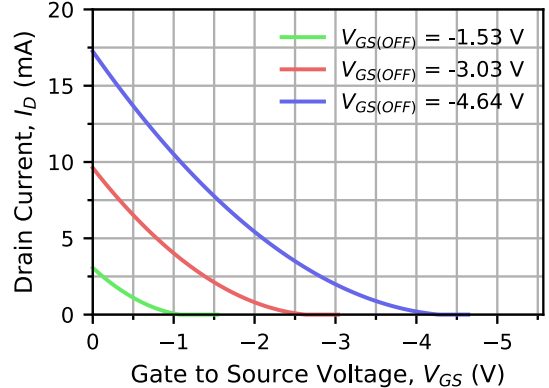
Typical Output @ $V_{GS(OFF)} = -3.03 \text{ V}$



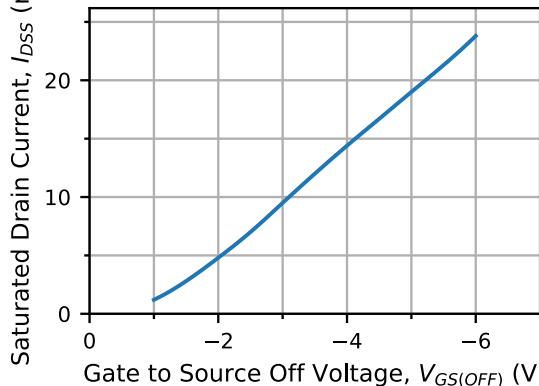
Typical Output @ $V_{GS(OFF)} = -4.64 \text{ V}$



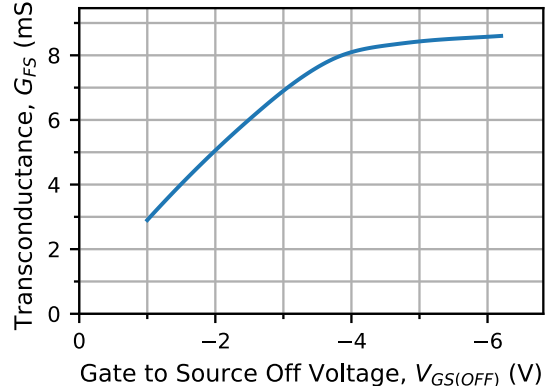
Typical Output I_D vs. V_{GS} @ $V_{DS} = 10 \text{ V}$



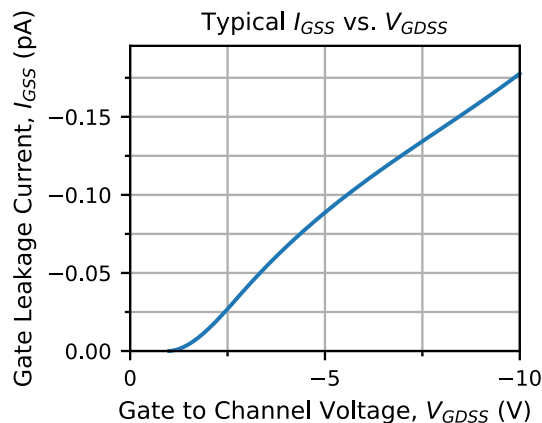
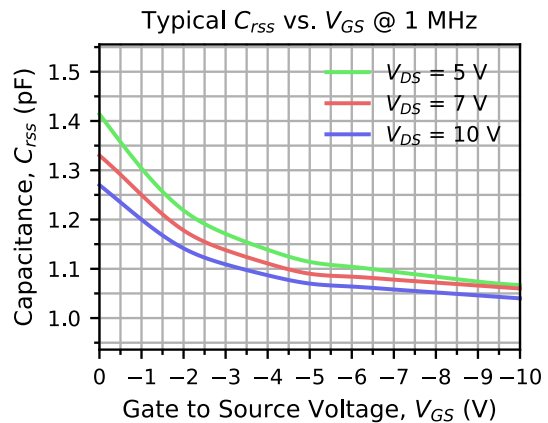
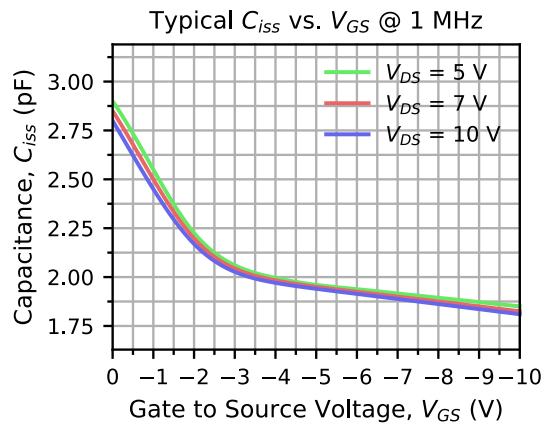
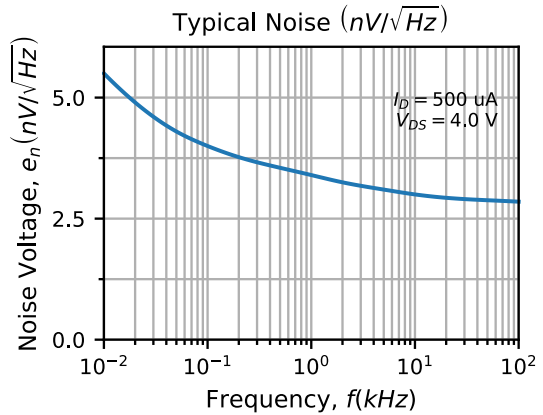
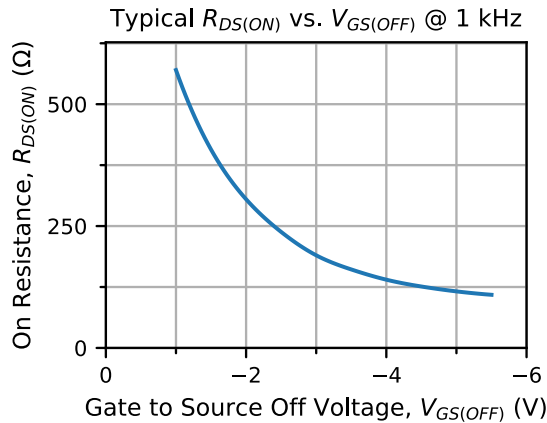
Typical I_{DSS} vs. $V_{GS(OFF)}$ @ $V_{DS} = 10 \text{ V}$



Typical G_{FS} vs. $V_{GS(OFF)}$

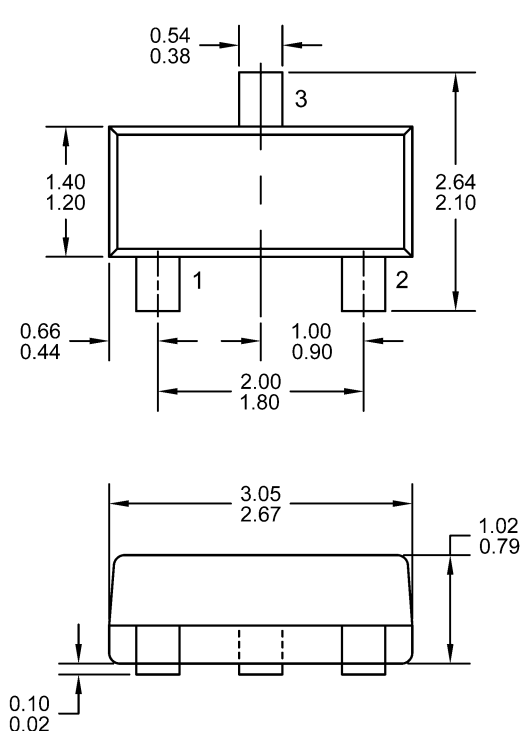


Typical IF150 Characteristics (Continued)



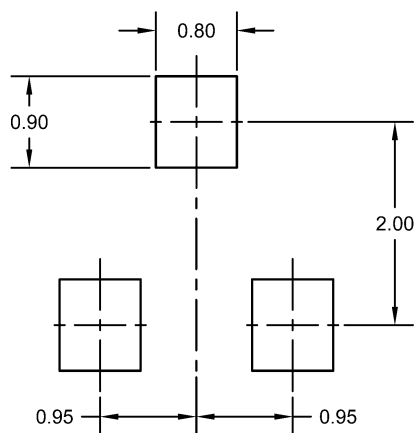
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

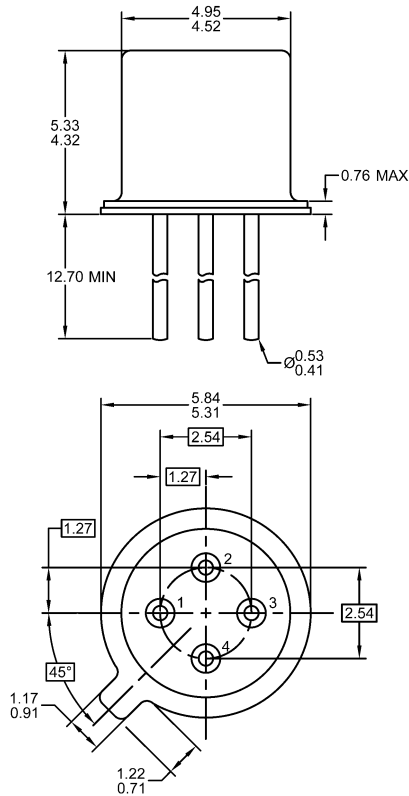
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

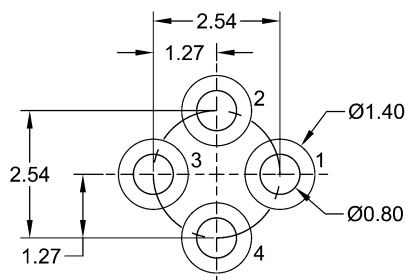
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit

www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	TBD	N/A	N/A
ESD	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM

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