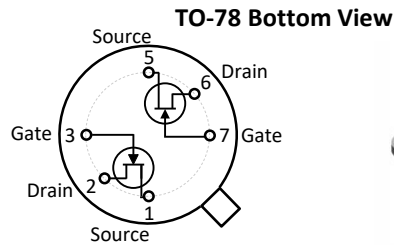


## IF3602 Dual Matched N-Channel JFET

### Features

- InterFET [N3600L Geometry](#)
- Ultra Low Noise: 0.3 nV/√Hz Typical
- High Gain: 750mS Typical
- Low  $R_{ds(on)}$ : 2.0 Ohms Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.



### Applications

- Low-Noise, High Gain Amplifiers
- Differential Amplifiers

### Description

The -20V InterFET IF3602 JFET is targeted for ultra low noise high gain differential amplifier designs. The IF3602 has a cutoff voltage of less than 2.0V ideal for low voltage applications. The TO-39 package is hermetically sealed and suitable for military applications.

### Product Summary

Parameters		IF3602 Min	Unit
$BV_{GSS}$	Gate to Source Breakdown Voltage	-20	V
$I_{DSS}$	Drain to Source Saturation Current	30	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.35	V
$G_{FS}$	Forward Transconductance	750	mS

### Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF3602T78	Through-Hole	TO-78	Bulk
IF3602COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IF3602CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



**Disclaimer:** It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

## Electrical Characteristics

### Maximum Ratings (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Value	Unit
$V_{RGS}$ Reverse Gate Source and Gate Drain Voltage	-20	V
$I_{FG}$ Continuous Forward Gate Current	10	mA
$P_D$ Continuous Device Power Dissipation	300	mW
$P$ Power Derating	4	mW/ $^\circ\text{C}$
$T_J$ Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
$T_{STG}$ Storage Temperature	-65 to 200	$^\circ\text{C}$

### Static Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

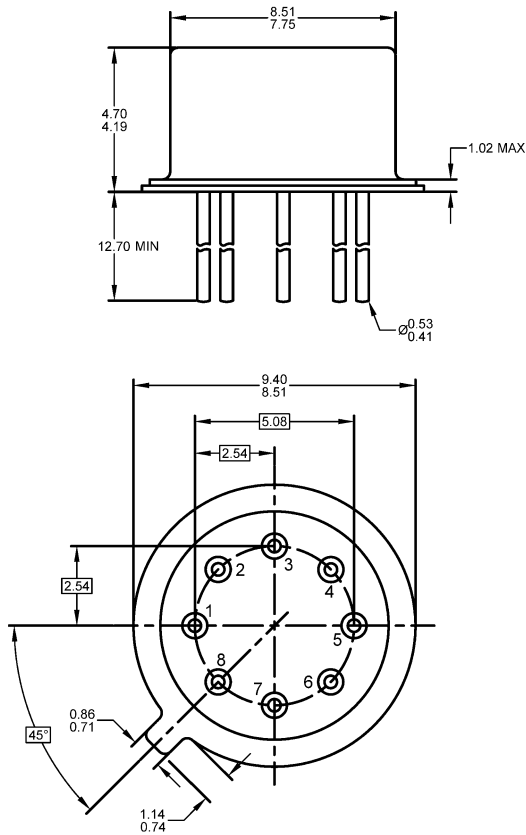
Parameters	Conditions	IF3602		Unit
		Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu\text{A}$	-20		V
$I_{GSS}$ Gate to Source Reverse Current	$V_{GS} = -10V, V_{DS} = 0V$		-0.5	nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10V, I_D = 0.5\text{nA}$	-0.35	-3	V
$I_{DSS}$ Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 10V$ (Pulsed)	30		mA

### Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Conditions	IF3602	Unit
		Typ	
$G_{FS}$ Forward Transconductance	$V_{DS} = 10V, V_{GS} = 0V, f = 1\text{kHz}$	750	mS
$C_{iss}$ Input Capacitance	$V_{DS} = 0V, V_{GS} = -4V, f = 1\text{MHz}$	300	pF
$C_{rss}$ Reverse Transfer Capacitance	$V_{DS} = 0V, V_{GS} = -4V, f = 1\text{MHz}$	200	pF
$e_n$ Equivalent Circuit Input Noise Voltage	$V_{DS} = 3V, I_D = 5\text{mA}, f = 100\text{Hz}$	0.3	$\text{nV}/\sqrt{\text{Hz}}$
$ V_{GS1} - V_{GS2} $ Differential Gate Source Voltage	$V_{DS} = 10V, I_D = 500\text{pA}$	100 (max)	mV

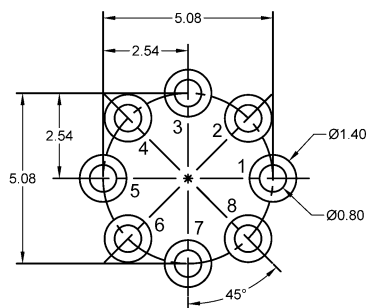
## TO-78 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 7.
4. Package weight approximately 0.44 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

### Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.