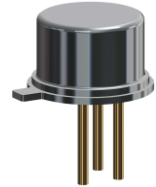
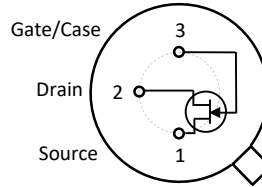


IF9030 N-Channel JFET

Features

- InterFET [N0903L Geometry](#)
- Low Noise: 0.7 nV/√Hz Typical
- High Gain: 150mS Typical
- Low Rds(on): 6.0 Ohms Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

TO-52 Bottom View



Applications

- Low-Noise, High Gain Amplifiers

Description

The -20V InterFET IF9030 JFET is targeted for low noise high gain amplifier designs. The IF9030 has a cutoff voltage of less than 2.0V ideal for low voltage applications. The TO-52 package is hermetically sealed and suitable for military applications.

Product Summary

Parameters		IF9030 Min	Unit
BV _{GSS}	Gate to Source Breakdown Voltage	-20	V
I _{DSS}	Drain to Source Saturation Current	30	mA
V _{GS(off)}	Gate to Source Cutoff Voltage	-0.35	V
G _{FS}	Forward Transconductance	80	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF9030T52	Through-Hole	TO-52	Bulk
IF9030COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IF9030CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG} Continuous Forward Gate Current	10	mA
P_D Continuous Device Power Dissipation	300	mW
P Power Derating	2.4	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 200	$^\circ\text{C}$

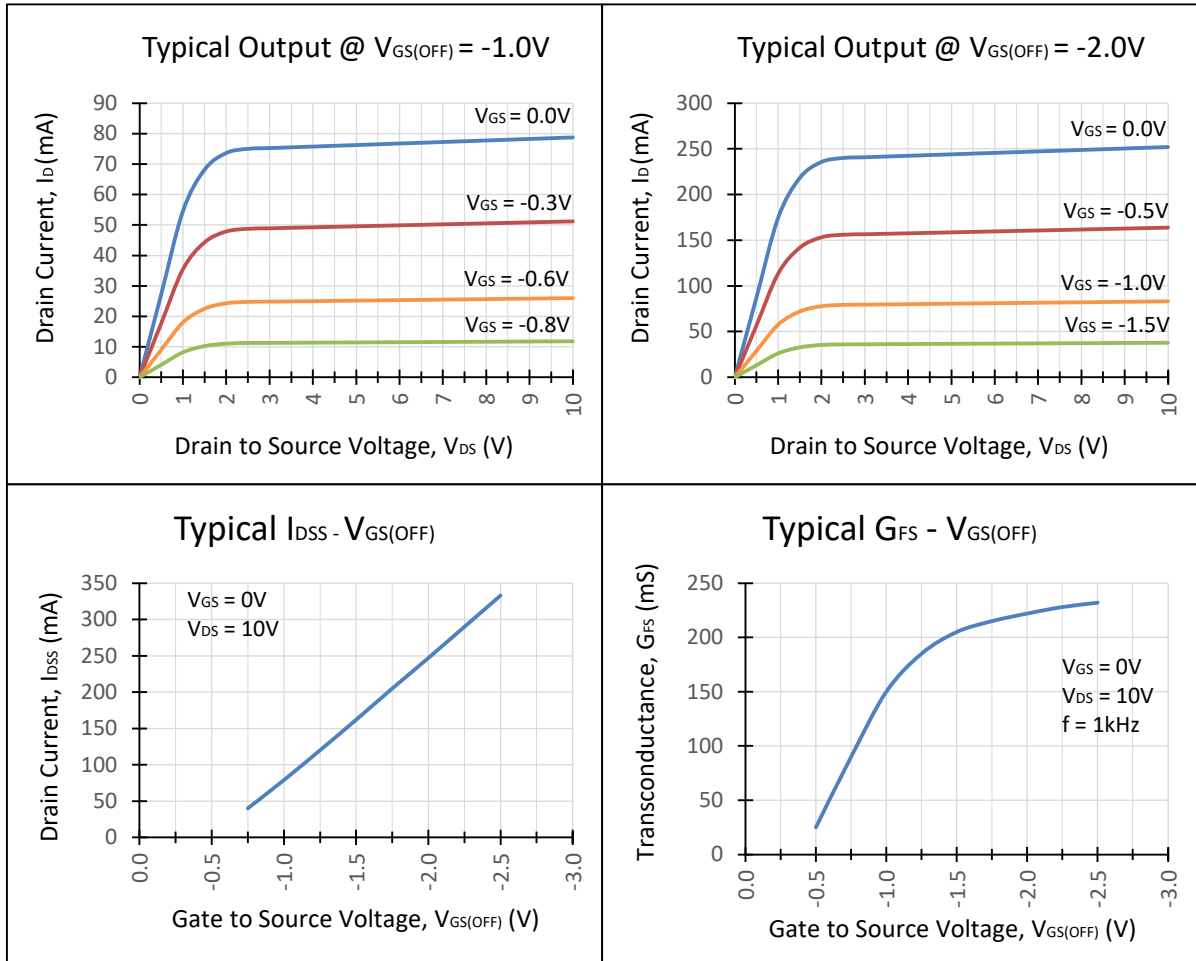
Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IF9030		Unit
		Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu\text{A}$	-20		V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -10V, V_{DS} = 0V$		-0.1	nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10V, I_D = 0.5\text{nA}$	-0.35	-2	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 10V$ (Pulsed)	30	300	mA

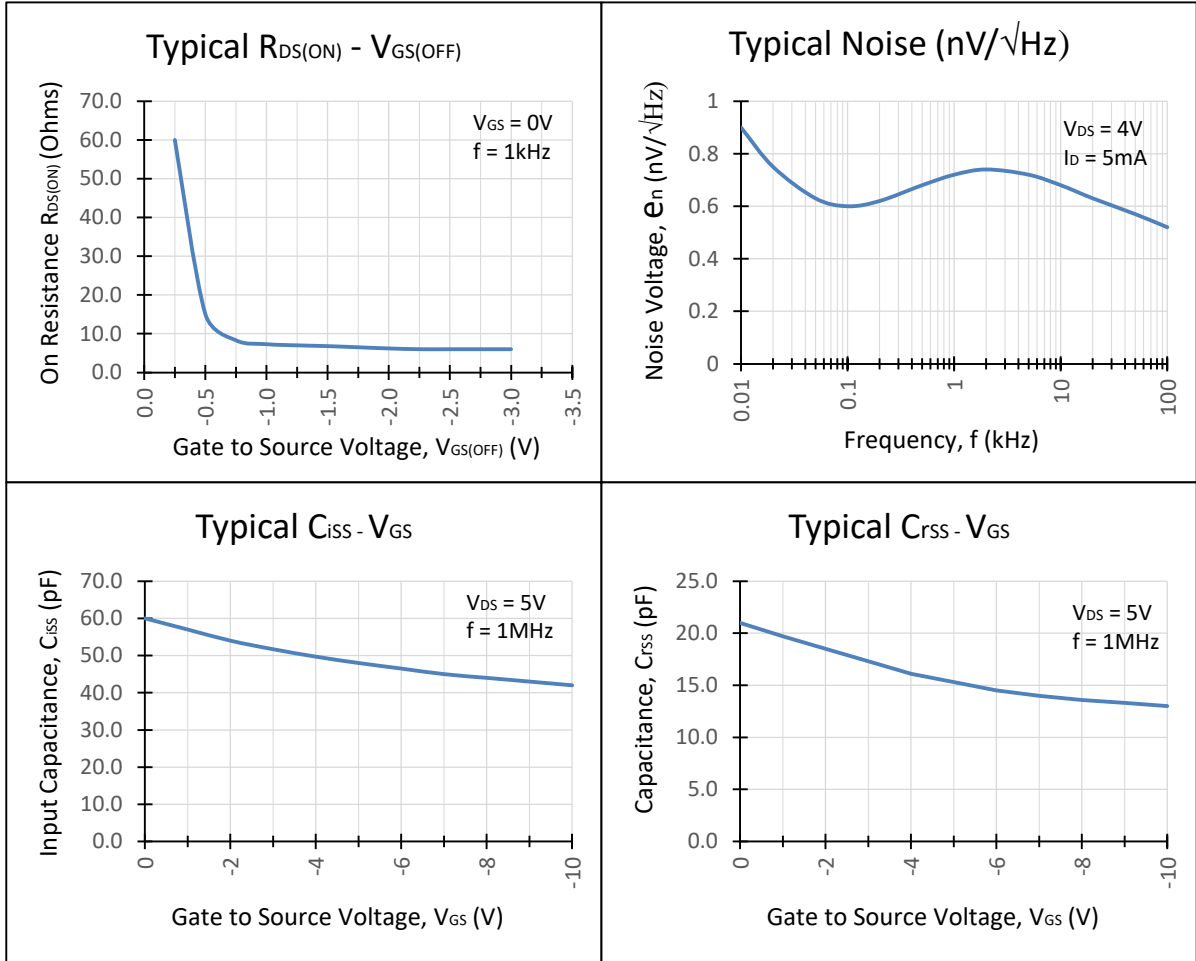
Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IF9030		Unit
		Min	Max	
G_{FS} Forward Transconductance	$V_{DS} = 10V, V_{GS} = 0V, f = 1\text{kHz}$	80		mS
C_{iss} Input Capacitance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{MHz}$		60	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 10V, I_D = 5\text{mA}, f = 1\text{MHz}$		20	pF
e_n Equivalent Circuit Input Noise Voltage	$V_{DS} = 4V, I_D = 5\text{mA}, f = 1\text{kHz}$	0.7 (typ)		$\text{nV}/\sqrt{\text{Hz}}$

Typical IF9030 Characteristics

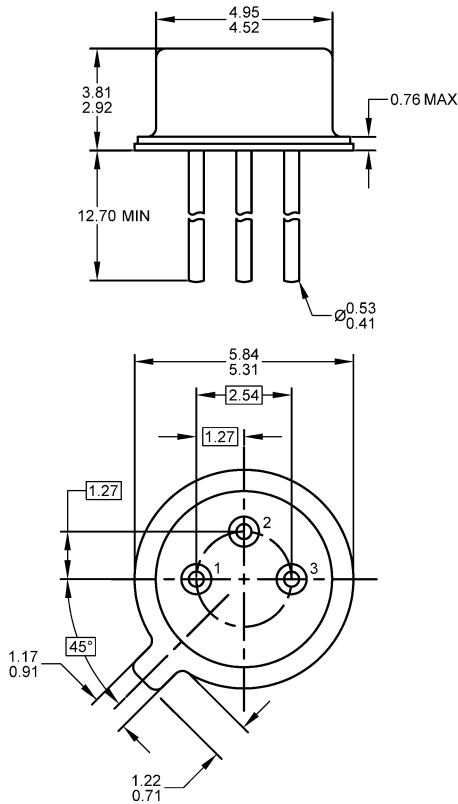


Typical IF9030 Characteristics (Continued)



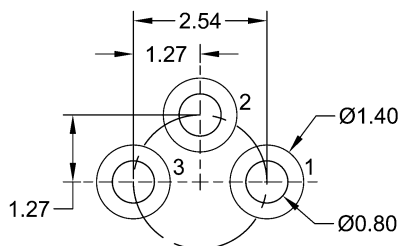
TO-52 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.26 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.