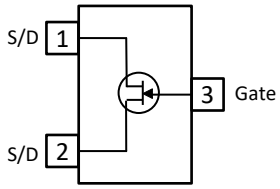
IFN3556, IFN3557 N-Channel JFET

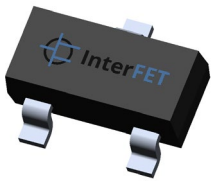
Features

- InterFET N0132L Geometry
- Low noise: 1.0 nV/√Hz typical
- High gain: 22mS typical
- Low gate leakage: 750fA typical @10V
- Low cutoff voltage: -1.0 typical
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT and bare die package options
- Edge case SPICE modeling: InterFET SPICE

SOT23 Top View



NOTE: S/D pins are interchangeable Source Drain connections



Industry Standard Crosses

- 2SK3557

InterFET Similar Parts

- IF1320

InterFET Dual Parts

- IF1322,IF1322A

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

InterFET's flagship low noise, low leakage N-CH JFET. High gain and high radiation tolerance for military and standard applications. The IFN3556 and IFN3557 have a cutoff voltage of less than -1.5V ideal for low-voltage supply applications. The InterFET proprietary JFET recipes result in highest radiation tolerance and lowest leakage JFETs on the market. Custom binning options available.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN3556ST3; IFN3557ST3	Surface Mount	SOT23	Bulk
IFN3556ST3TR; IFN3557ST3TR	7" Tape and Reel: 1,000 and 3,000 Pieces 13" Tape and Reel: 9000 Pieces	SOT23 SOT23	Minimum 1,000 Pieces Tape and Reel
IFN3556COT; IFN3557COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFN3556CFT; IFN3557CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		SOT-23	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation[1]	350	mW
P	Power Derating[1]	2.8	mW/°C
T_J	Operating Junction Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	°C

[1] Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	Min	Typ	Max	Unit
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA, V_{DS} = 0V	-20			V
I_{GSS}	Gate to Source Reverse Current	V_{DS} = 0V, V_{GS} = -10V		-0.75	-100	pA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 0.5 nA	-0.35		-1.5	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 10V, V_{GS} = 0V (Pulsed)	10*		32*	mA

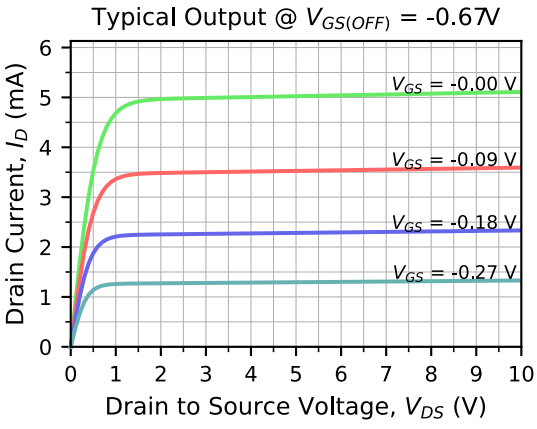
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

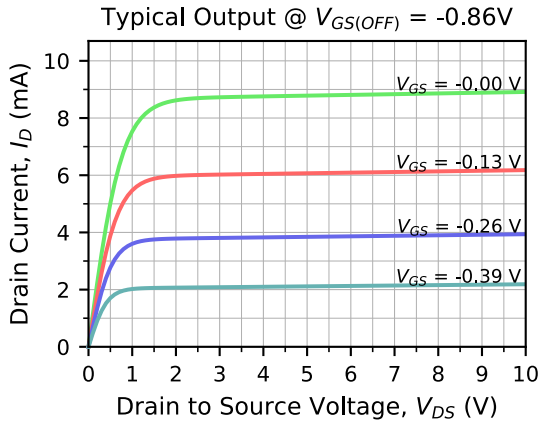
Parameters		Conditions	Min	Typ	Max	Unit
G_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 5 mA, f = 1kHz	15	22		mS
C_{iss}	Input Capacitance	V_{DS} = 10V, I_D = 5 mA, f = 1MHz			20	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 10V, I_D = 5 mA, f = 1MHz			5	pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 5 mA, f = 1kHz		1.0		nV/√Hz

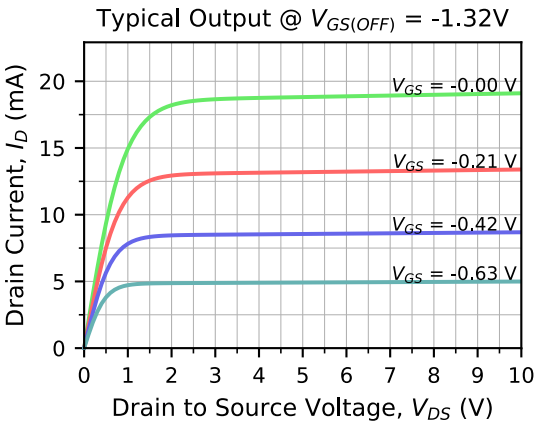
Class Characteristics (@ TA = 25°C, Unless otherwise specified)

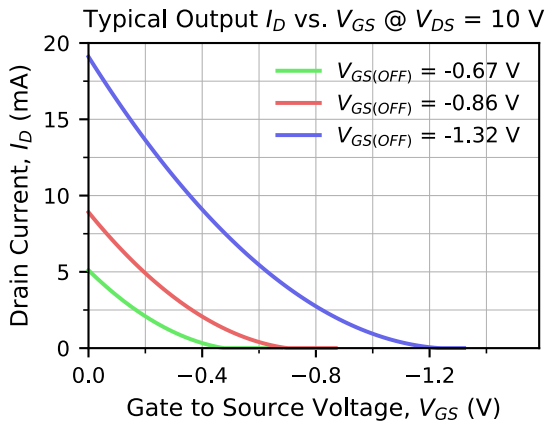
Rank	IFN3556	IFN3557
I_{DSS}	10.0 to 20.0	16.0 to 32.0

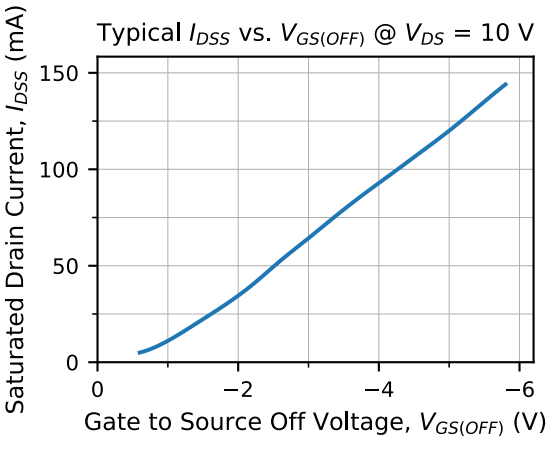
Typical IFN3556, IFN3557 Characteristics

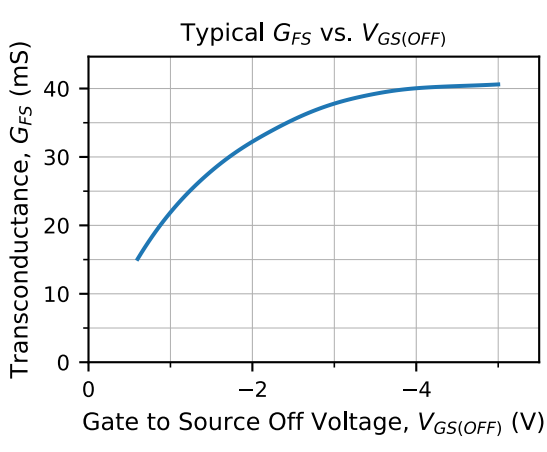




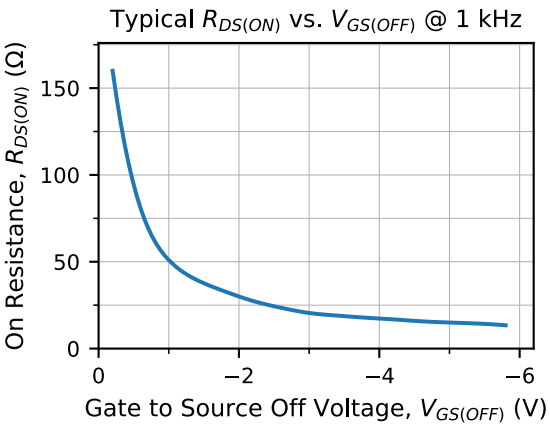


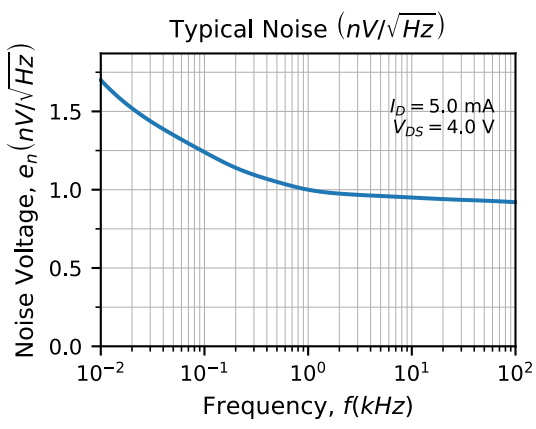


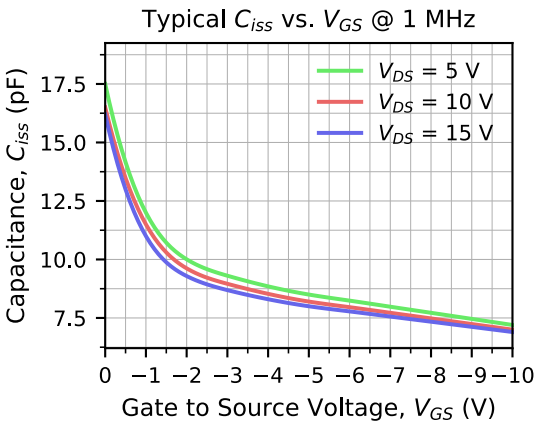


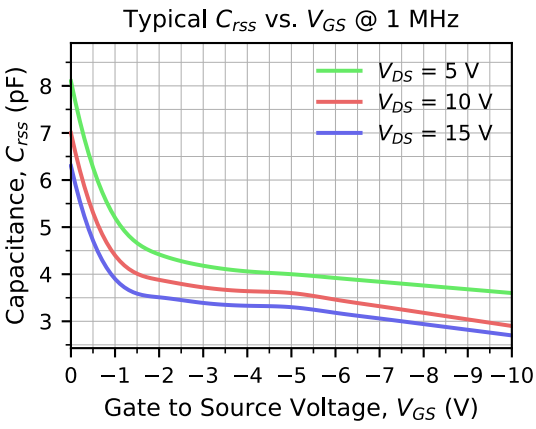


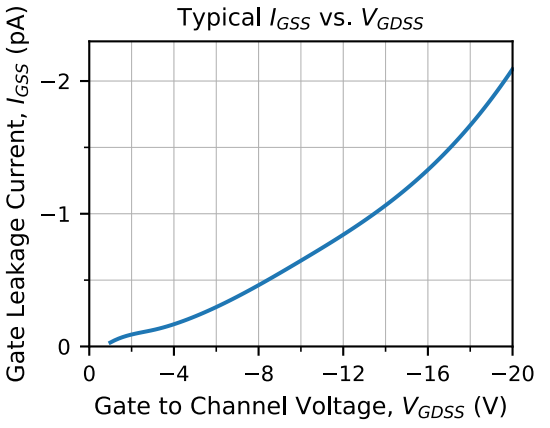
Typical IFN3556, IFN3557 Characteristics (Continued)





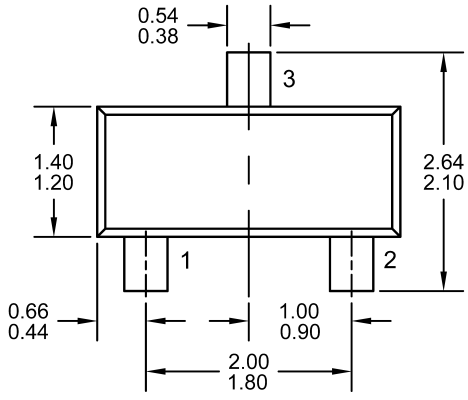


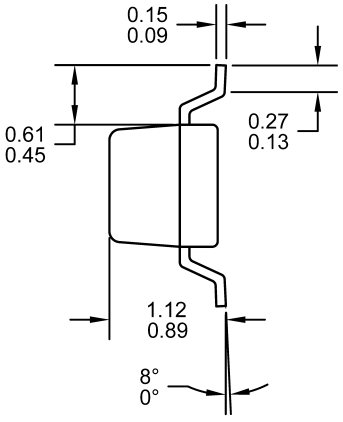


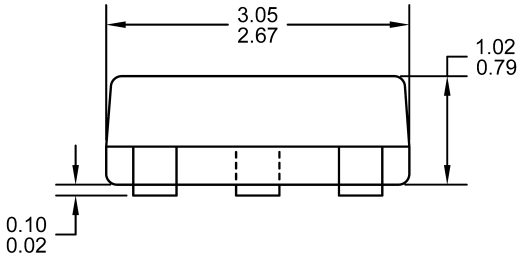


SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

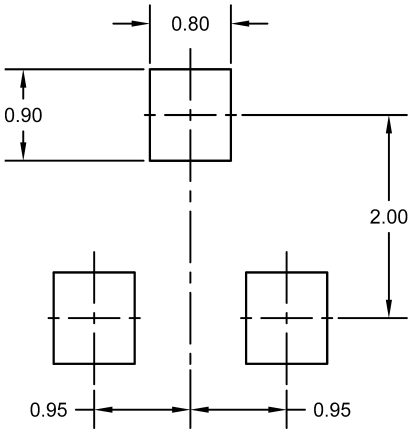






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.01 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 1	N/A	N/A
ESD	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM

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