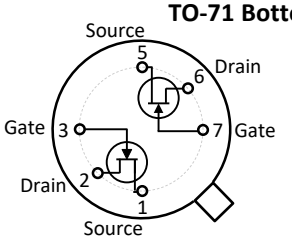
IFN860 Dual Matched N-Channel JFET

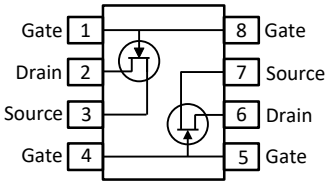
Features

- InterFET N0450L Geometry
- Low Noise: 0.9 nV/√Hz Typical
- High Gain: 75mS Typical
- Low Rds(on): 5.0 Ohms Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

TO-71 Bottom View



SOIC8 Top View



Applications

- Low-Noise Audio Amplifier
- Similar to Crystalonics CD860

Description

The -20V InterFET IFN860 JFET is targeted for low noise high gain amplifier stages for mid-frequencies designs. The TO-71 package is hermetically sealed and suitable for military applications.

Product Summary

Parameters		IFN860 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-20	V
I_{DSS}	Drain to Source Saturation Current	10	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.3	V
G_{FS}	Forward Transconductance	25	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN860	Through-Hole	TO-71	Bulk
SMP860	Surface Mount	SOIC8	Bulk
SMP860TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOIC8	Minimum 1,000 Pieces Tape and Reel
IFN860COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFN860CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	400	mW
P	Power Derating	2.3	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

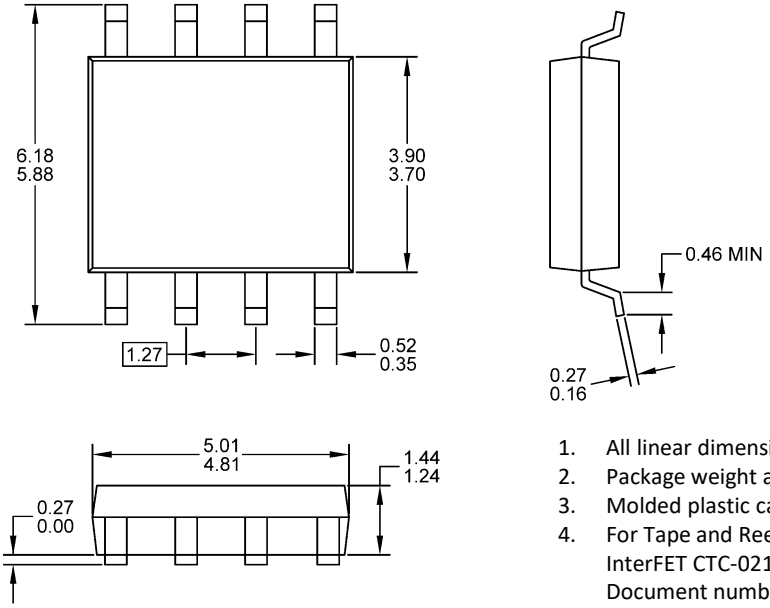
Parameters		Conditions	IFN860		Unit
			Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-20		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -10V, V_{DS} = 0V		3	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 100µA	-0.3	-3	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 10V (Pulsed)	10		mA
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 10V, I_D = 100µA		25	mV

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	IFN860			Unit
			Min	Typ	Max	
G_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = -10mA, f = 1kHz	25	40		mS
C_{iss}	Input Capacitance	V_{DS} = 10V, I_D = -10mA, f = 1MHz		30	35	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 10V, I_D = -10mA, f = 1MHz		17	20	pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DG} = 3V, I_D = 10mA, f = 1kHz			2	nV/√Hz

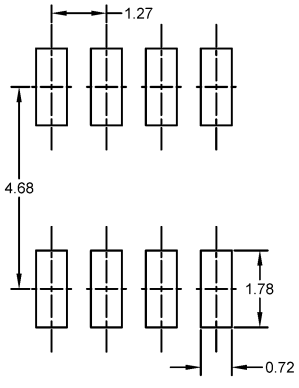
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

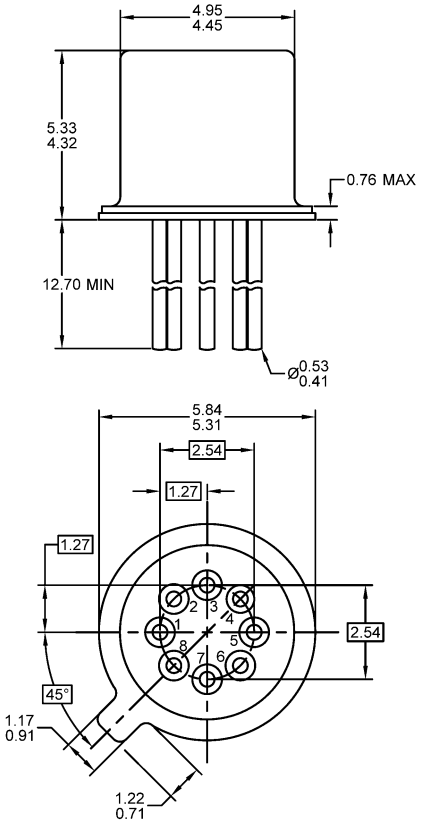
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

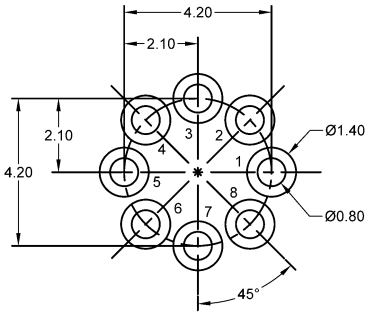
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.