

2N3819 N-Channel JFET

Features

- InterFET [N0032H Geometry](#)
- Low Noise: 7 nV/VHz Typical
- Low Ciss: 6pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

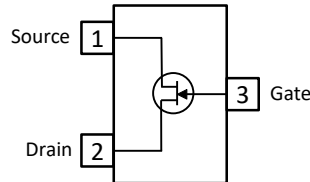
Applications

- Audio Amplifiers
- General Purpose Amplifiers
- Switches

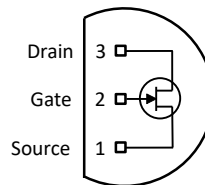
Description

The -25V InterFET 2N3819 JFET is targeted for low noise switching and audio amplifier applications. Gate leakages are typically less than 10pA at room temperatures.

SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters		2N3819 Min	Unit
BV _{GSS}	Gate to Source Breakdown Voltage	25	V
I _{DSS}	Drain to Source Saturation Current	2	mA
V _{GS(off)}	Gate to Source Cutoff Voltage	8 (Max)	V
G _{FS}	Forward Transconductance	2000	μmhos

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N3819	Through-Hole	TO-92	Bulk
SMP3819	Surface Mount	SOT23	Bulk
SMP3819TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N3819COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N3819CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	25	V
I_{FG} Continuous Forward Gate Current	10	mA
P_D Continuous Device Power Dissipation	350	mW
P Power Derating	2.8	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-55 to 150	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

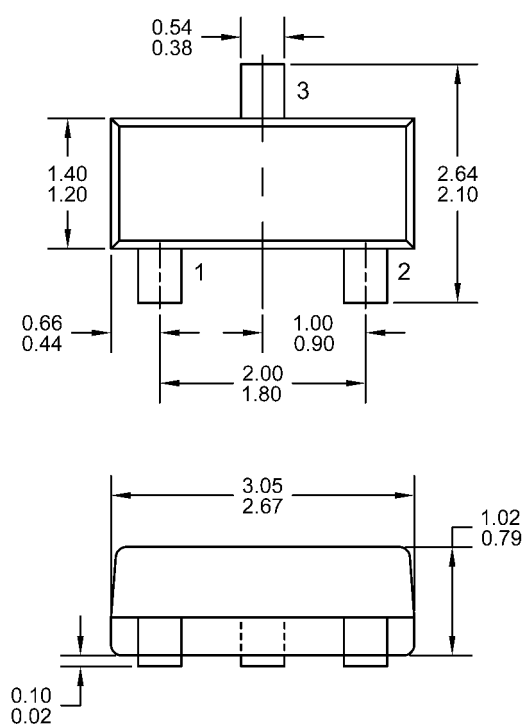
Parameters	Conditions	2N3819		Unit
		Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = 1\mu A$	-25		V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -15V, V_{DS} = 0V$		2	nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 15V, I_D = 2nA$		8	V
V_{GS} Gate to Source Voltage	$V_{DS} = 15V, I_D = 200\mu A$	-0.5	-7.5	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 15V$ (Pulsed)	2	20	mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N3819		Unit
		Min	Max	
G_{FS} Forward Transconductance	$V_{DS} = 15V, V_{GS} = 0V, f = 1kHz$	2000	6500	μmhos
G_{OS} Output Conductance	$V_{DS} = 15V, V_{GS} = 0V, f = 1kHz$		50	μmhos
C_{iss} Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1kHz$		8	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1kHz$		4	pF

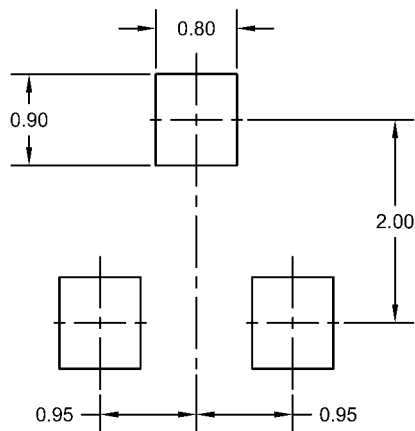
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

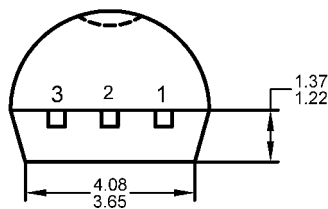
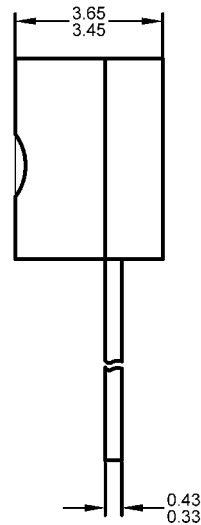
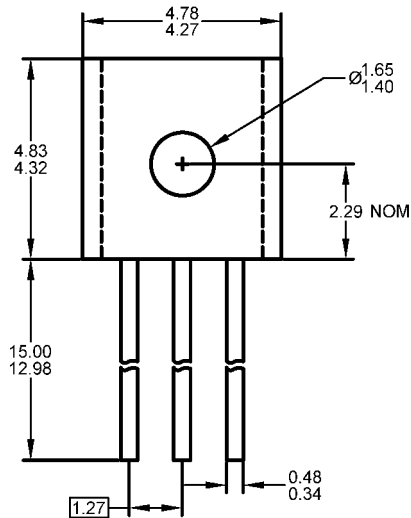
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

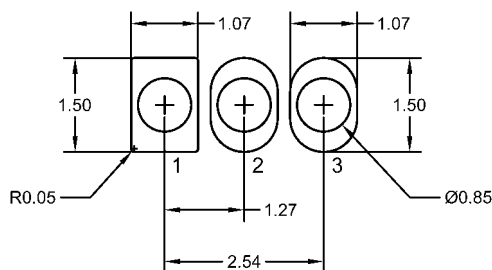
TO-92 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.