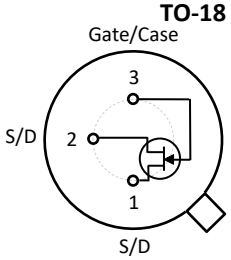
2N4091, 2N4092, 2N4093 N-Channel JFET
Jan Equivalent Parts

Features

- InterFET N0132S Geometry
- Low noise: 1.0 nV/√Hz typical
- High gain: 22mS typical
- Low gate leakage: 750fA typical @20V
- Typical $V_{GS(OFF)}$: -2.5V
- Typical I_{DSS}: 12mA
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- Edge case SPICE modeling: InterFET SPICE

TO-18 Bottom View



Built to MIL-PRF-19500

(S/D pins are interchangeable)

Industry Standard Crosses

- TBD

InterFET Similar Parts

- J112, 113A
- 2N4860-1, 2N4857-8-9, 2N4392, 2N3971

Applications

- General: Amplifiers; Switches; Voltage regulators;
- Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The -40V InterFET 2N4091, 2N4092, and 2N4093 JFET's are targeted for very low noise switching applications for mid to high frequency designs. Gate leakages are typically 50pA at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N4091JANequiv, 2N4092JANequiv, 2N4093JANequiv	JAN equivalent	TO-18	Bulk
2N4091JANTXequiv, 2N4092JANTXequiv, 2N4093JANTXequiv	JANTX equivalent	TO-18	Bulk
2N4091JANTXVequiv, 2N4092JANTXVequiv, 2N4093JANTXVequiv	JANTXV equivalent	TO-18	Bulk
2N4091JANSequiv, 2N4092JANSequiv, 2N4093JANSequiv	JANS equivalent	TO-18	Bulk

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		TO-18	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation[1]	500	mW
P	Power Derating[1]	3.3	mW/°C
T_J	Operating Junction Temperature	-65 to 175	°C
T_{STG}	Storage Temperature	-65 to 175	°C

[1] Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

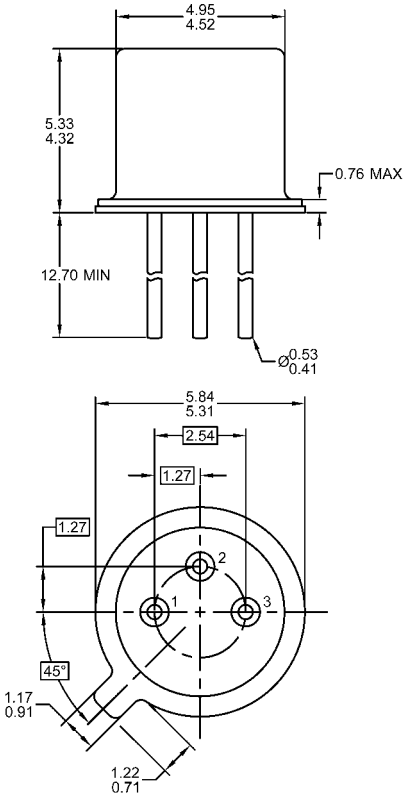
Parameters		Conditions	2N4091		2N4092		2N4093		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-40		-40		-40		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V		-1		-1		-1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA	-5	-10	-2	-7	-1	-5	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 20V (Pulsed)	30		15		8		mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	2N4091		2N4092		2N4093		Unit
			Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{GS} = 0V, I_D = 0A, f = 1kHz		30		50		80	Ω
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		16		16		16	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 0V, V_{GS} = -20V, f = 1MHz		5		5		5	pF
t_d	Turn-On Delay Time	V_{DD} = 3V, $V_{GS(ON)}$ = 0V		10		15		20	ns
t_r	Rise Time	V_{DD} = 3V, $V_{GS(ON)}$ = 0V		10		20		40	ns
t_{off}	Turn-Off Time	V_{DD} = 3V,$V_{GS(ON)}$ = 0V		40		60		80	ns

TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

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