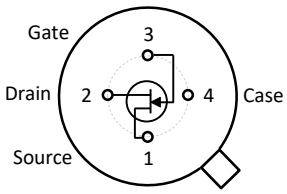
2N4220/A, 2N4221/A N-Channel JFET

Features

- InterFET N0016H Geometry
- Typical Noise: 6 nV/√Hz
- Low Ciss: 3.5pF Typical
- High Input Impedance
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

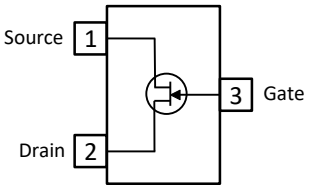
TO-72 Bottom View



Applications

- Mixers
- Oscillators
- Small Signal Amplifier
- VHF Amplifiers

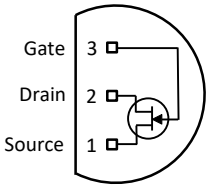
SOT23 Top View



Description

The -50V InterFET 2N4220/A and 2N4221/A are targeted for sensitive amplifier stages for mid-frequencies designs. Gate leakages are typically less than 10pA at room temperatures. The “A” variants are screened for lower noise. The TO-72 package is hermetically sealed and suitable for military applications.

TO-92 Bottom View



Product Summary

Parameters		2N4220/A Min	2N4221/A Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-30	-30	V
I_{DSS}	Drain to Source Saturation Current	0.5	2	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage			V
G_{FS}	Forward Transconductance	1000	2000	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N4220; 2N4221 2N4220A; 2N4221A	Through-Hole	TO-72	Bulk
PN4220; PN4221 PN4220A; PN4221A	Through-Hole	TO-92	Bulk
SMP4220; SMP4221 SMP4220A; SMP4221A	Surface Mount	SOT23	Bulk
SMP4220TR; SMP4221TR SMP4220ATR; SMP4221ATR	7“ Tape and Reel: Max 3,000 Pieces 13” Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N4220COT; 2N4221COT 2N4220ACOT; 2N4221ACOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N4220CFT; 2N4221CFT 2N4220ACFT; 2N4221ACFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-30	V
I_{FG}	Continuous Forward Gate Current	10	mA
P_D	Continuous Device Power Dissipation	300	mW
P	Power Derating	2	mW/°C
T_J	Operating Junction Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 175	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified, Highlighted values = A variant)

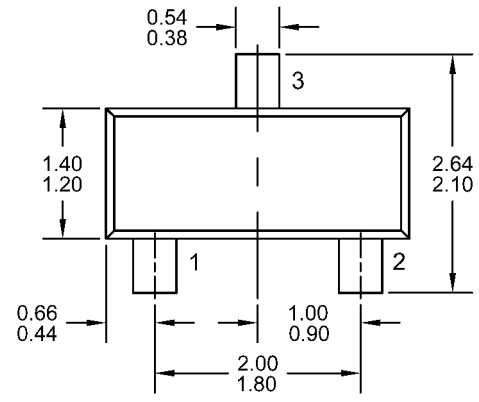
Parameters		Conditions	2N4220/A		2N4221/A		Unit
			Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-30		-30		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -15V, V_{DS} = 0V, T_A = 25°C		-0.1		-0.1	nA
		V_{GS} = -15V, V_{DS} = 0V, T_A = 150°C		-0.1		-0.1	µA
V_{GS}	Gate to Source Voltage	V_{DS} = 15V, I_D = ( )	-0.5 (50)	-2.5 (50)	-1 (200)	-5 (200)	V µA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.1nA		-4		-6	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 15V (Pulsed)	0.5	3	2	6	mA

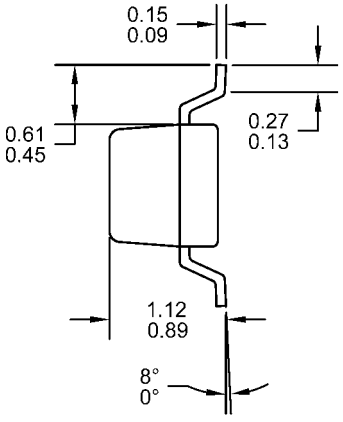
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified, Highlighted values = A variant)

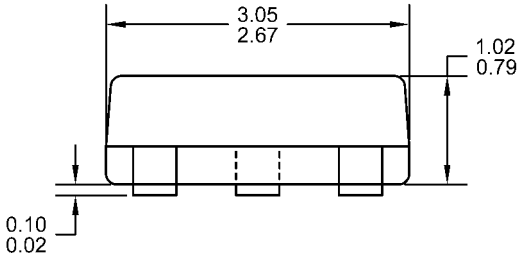
Parameters		Conditions	2N4220/A		2N4221/A		Unit
			Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = 15V, V_{GS} = 0V, f = 1kHz	1000	4000	2000	5000	µS
G_{OS}	Output Conductance	V_{DS} = 15V, V_{GS} = 0V, f = 1kHz		10		20	µS
$\|Y_{fs}\|$	Forward Transmittance	V_{DS} = 15V, V_{GS} = 0V, f = 100MHz	750		750		µS
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		6		6	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		2		2	pF
NF	Noise Figure	V_{DS} = 15V, V_{GS} = 0V, f = 100Hz					dB
		R_G = 1 MΩ		2.5		2.5	

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

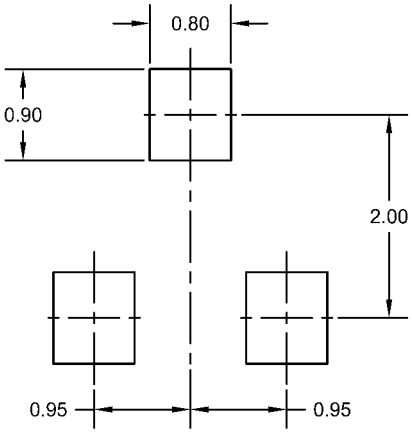






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

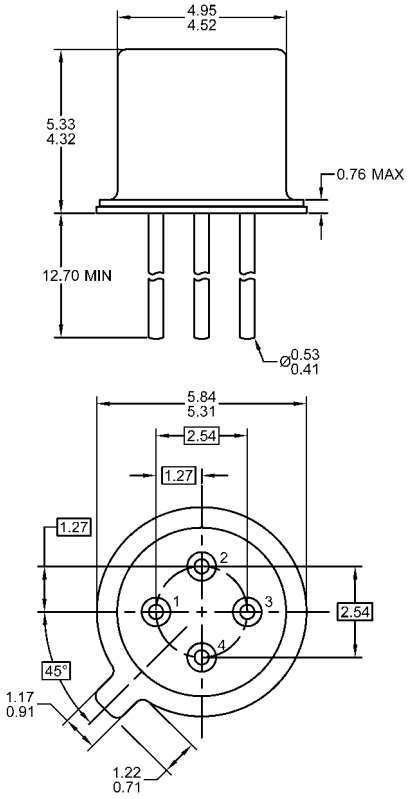
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

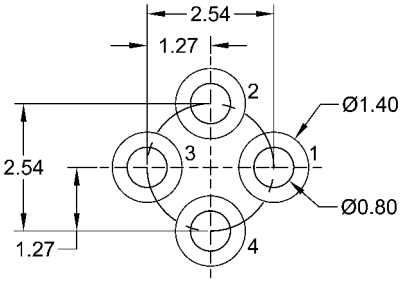
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

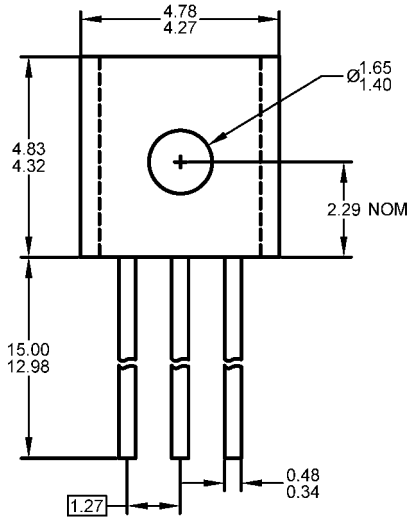
Suggested Through-Hole Layout

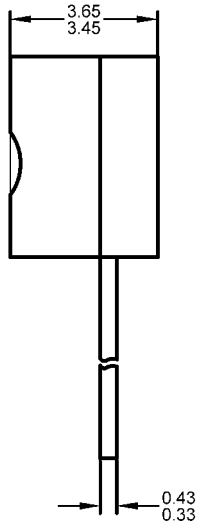


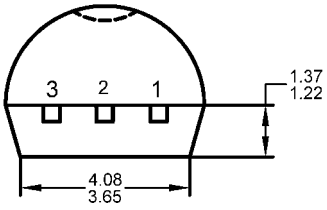
1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

TO-92 Mechanical and Layout Data

Package Outline Data

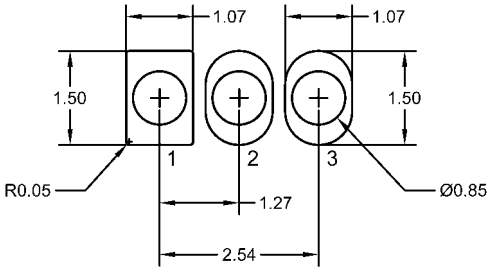






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.