

2N4338, 2N4339 N-Channel JFET

Features

- InterFET [N0016H Geometry](#)
- Low gate leakage: < 1pA typical @40V
- Low Ciss: 3pF typical
- Typical noise: 3.5 nV/√Hz
- Low $V_{GS(OFF)}$: < -1.0V for 2N4338
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: [InterFET SPICE](#)

Industry Standard Crosses

- 2N3460, 2N3969, 2N4220, 2N4867, 2N4868
- MMBFJ201, MMBFJ202, SST201, SST202, SST230

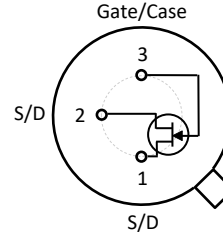
InterFET Similar Parts

- IFN201, IFN201A, IFN202, IFN160A
- SMP3460, SMP3969, SMP4220, SMP4867, SMP4868
- J201, J202, J230, SMPJ201, SMPJ202, SMPJ230

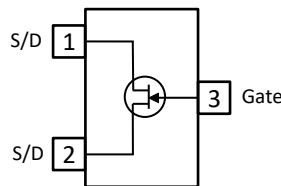
InterFET Dual Parts

- IFNU231, IFNU232, IFNU233, IFNU234, IFNU235
- IFN5197, IFN5198, IFN5199, IFNU410, IFNU411, IFNU412

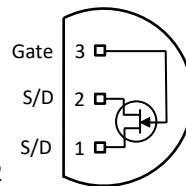
TO-18 Bottom View



SOT23 Top View



TO-92 Bottom View



NOTE: S/D pins are interchangeable Source Drain connections

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone preamplifiers
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The -50V InterFET 2N4338 and 2N4339 are very low leakage low input capacitance N-channel JFETs for low noise precision amplifier stages. Gate leakages are typically less 750fA at room temperatures. The 2N4338 has a cutoff voltage of less than -1.0V ideal for low-level power supplies. Proprietary InterFET processes yield exceptionally high radiation tolerance.

Ordering Information

Part Number	Description	Case	Packaging
2N4338; 2N4339	Through-Hole	TO-18	Bulk
PN4338; PN4339	Through-Hole	TO-92	Bulk
SMP4338; SMP4339	Surface Mount	SOT23	Bulk
SMP4338TR; SMP4339TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N4338COT; 2N4339COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N4338CFT; 2N4339CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	TO-18	SOT-23	TO-92	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-30	-30	-30	V
I_{FG} Continuous Forward Gate Current	50	50	50	mA
P_D Continuous Device Power Dissipation ¹	500	350	500	mW
P Power Derating ¹	3.3	2.8	4	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 175	-55 to 150	-55 to 150	$^\circ\text{C}$

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

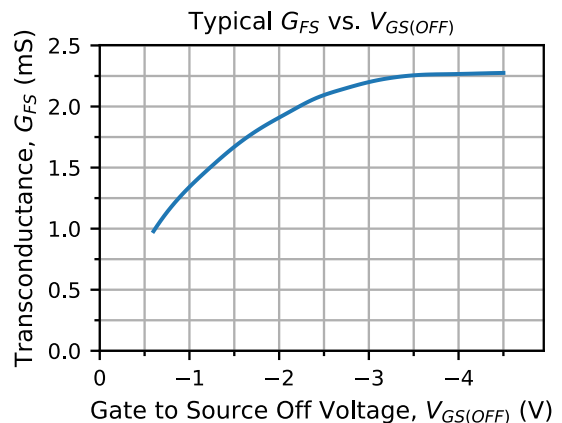
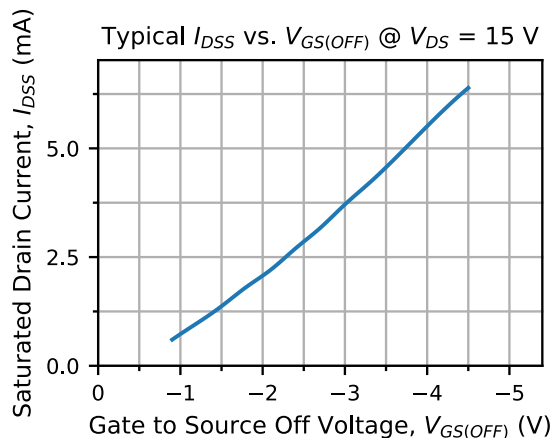
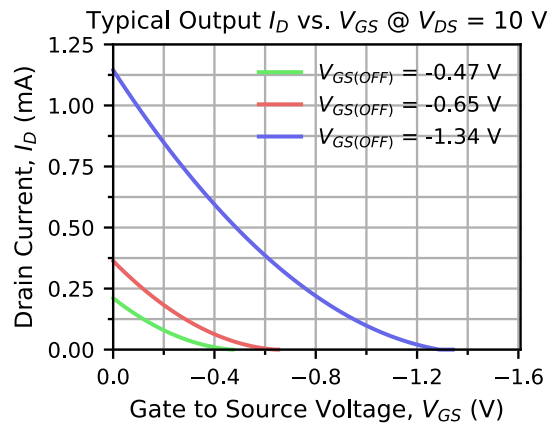
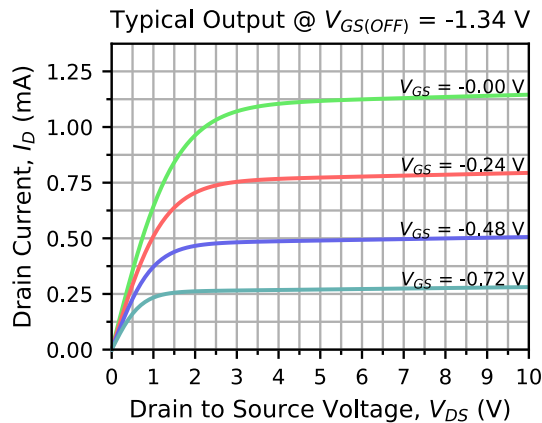
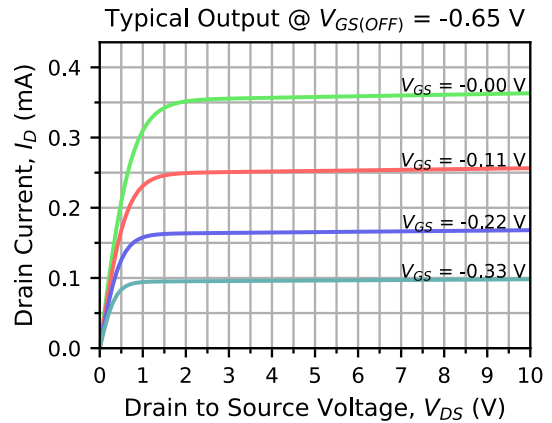
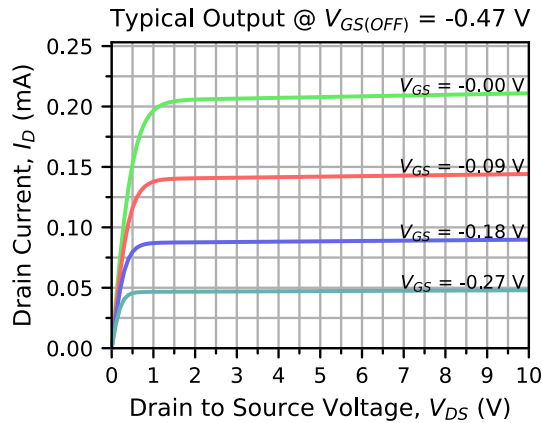
Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N4338		2N4339		Unit
		Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu A$	-50		-50		V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -30V, V_{DS} = 0V, T_A = 25^\circ\text{C}$ $V_{GS} = -30V, V_{DS} = 0V, T_A = 150^\circ\text{C}$		-0.1 -100		-0.1 -100	nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 15V, I_D = 0.1\mu A$	-0.3	-1.0	-0.6	-1.8	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 15V$ (Pulsed)	0.2	0.6	0.5	1.5	mA
$I_{D(OFF)}$ Drain Cutoff Current	$V_{DS} = 15V, V_{GS} = -5V$		0.05		0.05	nA

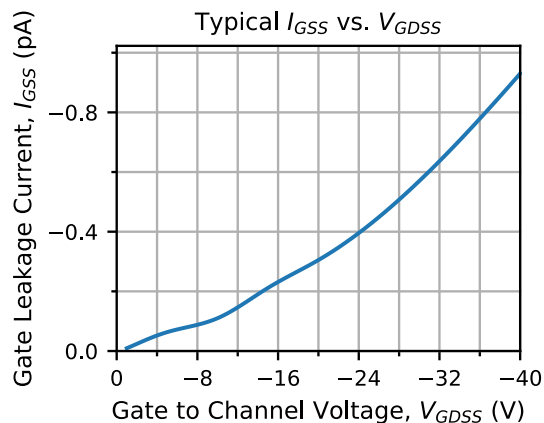
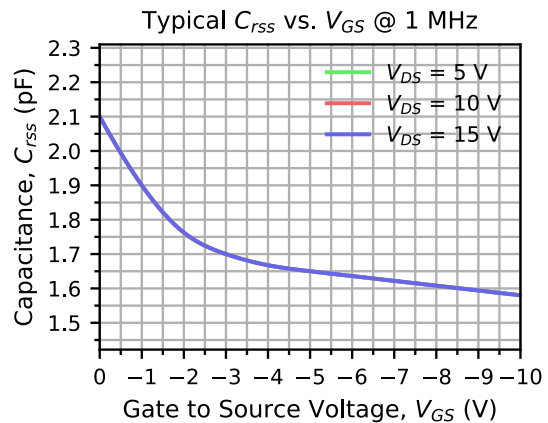
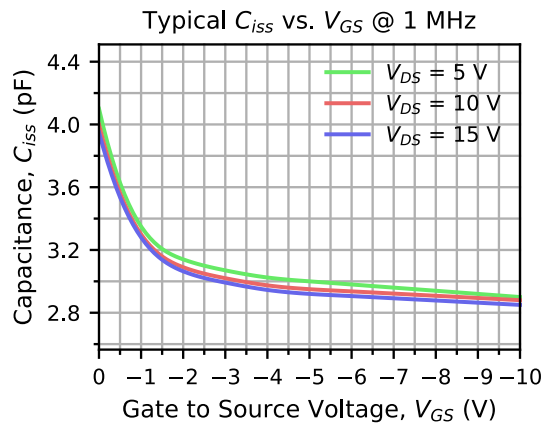
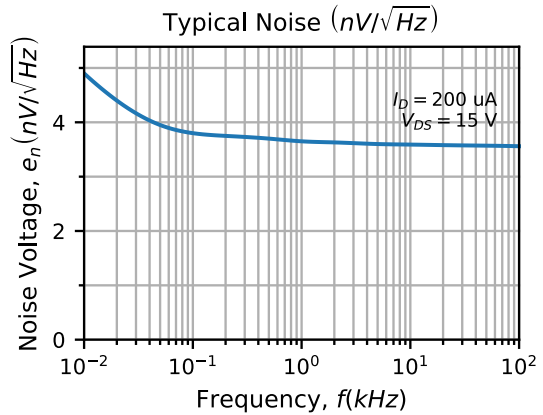
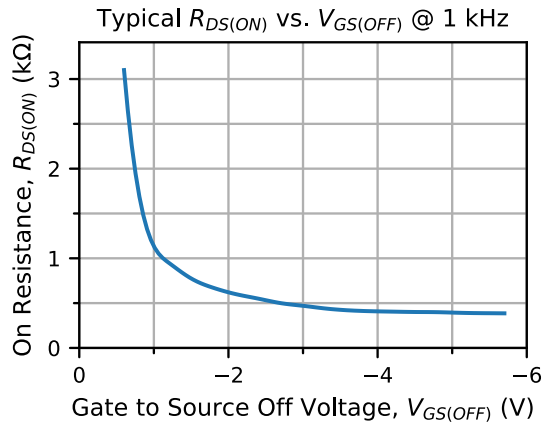
Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N4338		2N4339		Unit
		Min	Max	Min	Max	
G_{FS} Forward Transconductance	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{kHz}$	600	1800	800	2400	μS
G_{OS} Output Conductance	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{kHz}$		5		15	μS
$R_{DS(ON)}$ Drain to Source ON Resistance	$V_{GS} = 0V, I_D = 0A, f = 1\text{kHz}$		2500		1700	Ω
C_{iss} Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{MHz}$		7		7	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{MHz}$		3		3	pF
NF Noise Figure	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{kHz}$ $R_G = 1\text{M}\Omega, BW = 200\text{Hz}$		1		1	dB

Typical 2N4338, 2N4339 Characteristics

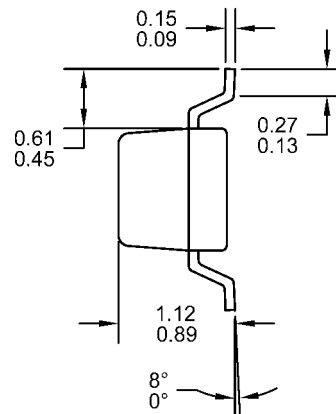
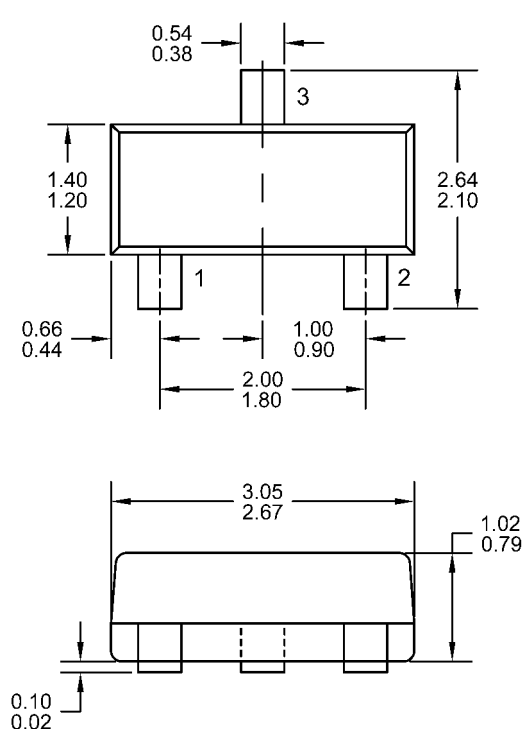


Typical 2N4338, 2N4339 Characteristics (Continued)



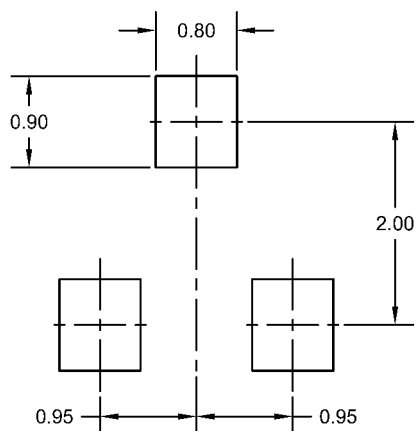
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

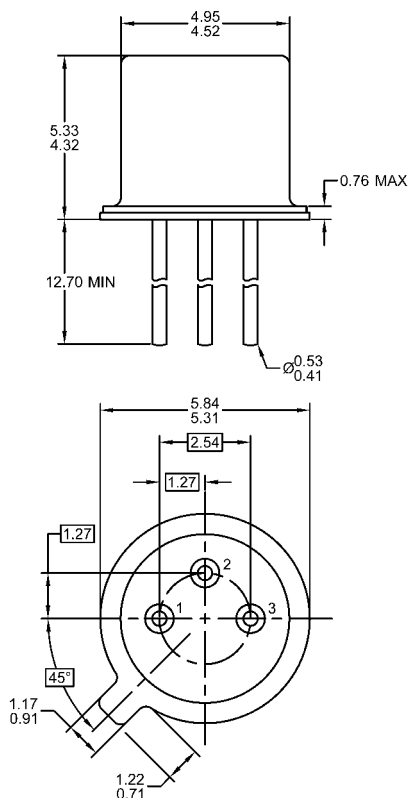
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

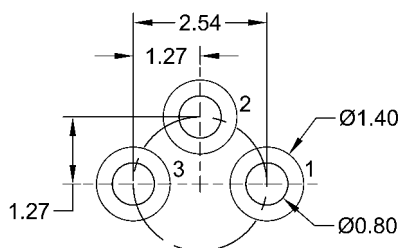
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

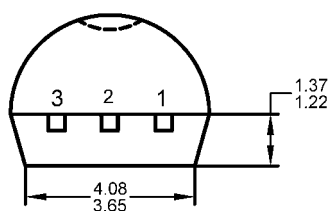
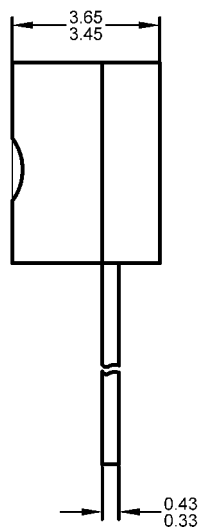
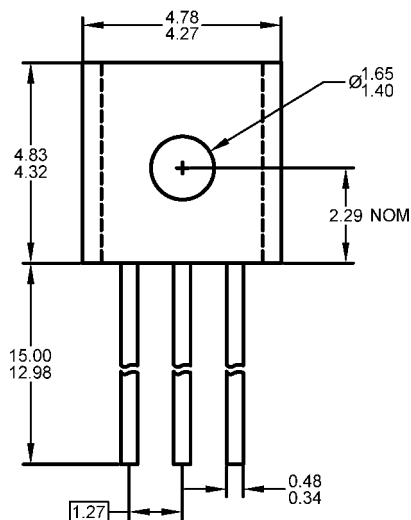
Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

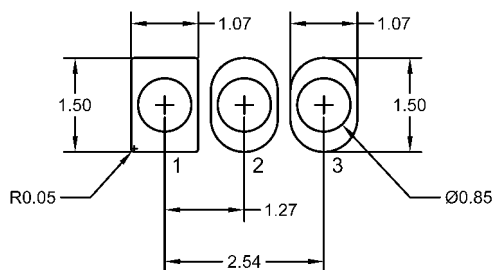
TO-92 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit

www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 1	N/A	N/A
ESD	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM

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