2N4856/A, 2N4857/A, 2N4858/A N-Channel JFET

Features

- InterFET N0132S Geometry
- Low Noise: 1.2 nV/√Hz Typical
- Fast Switching
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

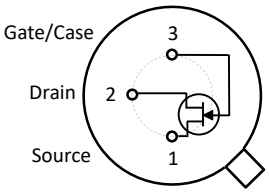
Applications

- Choppers
- Commutators
- Analog Switches

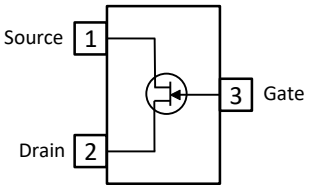
Description

The -40V InterFET 2N4856/A, 2N4857/A, and 2N4858/A JFET's are targeted for very low noise switching applications for mid to high frequency designs. Gate leakages are typically 50pA at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications.

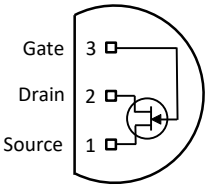
TO-18 Bottom View



SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters		2N4856/A Min	2N4857/A Min	2N4858/A Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-40	-40	-40	V
I_{DSS}	Drain to Source Saturation Current	50	20	8	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-4	-2	-0.8	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N4856; 2N4857; 2N4858 2N4856A; 2N4857A; 2N4858A	Through-Hole	TO-18	Bulk
PN4856; PN4857; PN4858 PN4856A; PN4857A; PN4858A	Through-Hole	TO-92	Bulk
SMP4856; SMP4857; SMP4858 SMP4856A; SMP4857A; SMP4858A	Surface Mount	SOT23	Bulk
SMP4856TR; SMP4857TR; SMP4858TR SMP4856ATR; SMP4857ATR; SMP4858ATR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N4856COT; 2N4857COT; 2N4858COT 2N4856ACOT; 2N4857ACOT; 2N4858ACOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N4856CFT; 2N4857CFT; 2N4858CFT 2N4856ACFT; 2N4857ACFT; 2N4858ACFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	1800	mW
P	Power Derating	10	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified, Highlighted values = A variant)

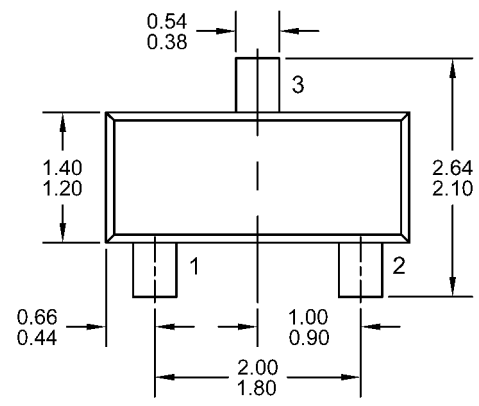
Parameters		Conditions	2N4856/A		2N4857/A		2N4858/A		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA,V_{DS} = 0V	-40		-40		-40		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V, T_A = 25°C V_{GS} = -20V, V_{DS} = 0V, T_A = 150°C		-250 -500		-200 -500		-200 -500	pA nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.5nA	-4	-10	-2	-6	-0.8	-4	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 15V, V_{GS} = 0V (Pulsed)	50		20	100	8	80	mA
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = 15V, V_{GS} = -10V, T_A = 25°C V_{DS} = 15V, V_{GS} = -10V, T_A = 150°C		250 500		250 500		250 500	pA nA
$V_{DS(ON)}$	Drain to Source ON Voltage	V_{GS} = 0V, I_D = ( )		0.75 (20)		0.5 (10)		0.5 (5)	V mA

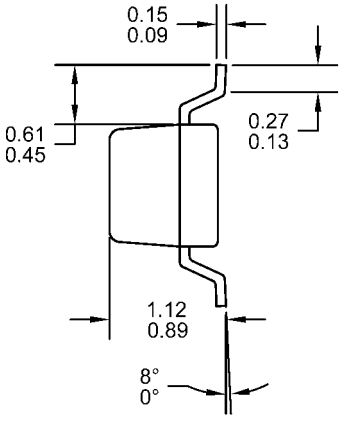
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified, Highlighted values = A variant)

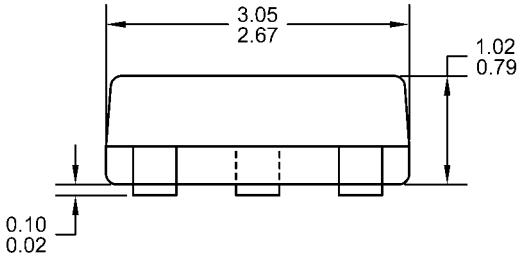
Parameters		Conditions	2N4856/A		2N4857/A		2N4858/A		Unit
			Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{GS} = 0V, I_D = 0A, f = 1kHz		25		40		60	Ω
C_{iss}	Input Capacitance	V_{DS} = 0V, V_{GS} = -10V, f = 1MHz		18		18		18	pF
				10		10		10	
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 0V, V_{GS} = -10V, f = 1MHz		8		8		8	pF
				4		3.5		3.5	
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10V, $V_{GS(ON)}$ = 0V $I_{D(ON)}$ = ( ), $V_{GS(OFF)}$ = [ ]		6		6		10	ns
				5		6		8	
				(20) [-10]		(10) [-6]		(5) [-4]	(mA) [V]
t_r	Rise Time	V_{DD} = 10V, $V_{GS(ON)}$ = 0V $I_{D(ON)}$ = ( ), $V_{GS(OFF)}$ = [ ]		3		4		10	ns
				3		4		8	
				(20) [-10]		(10) [-6]		(5) [-4]	(mA) [V]
$t_{d(off)}$	Turn-Off Delay Time	V_{DD} = 10V, $V_{GS(ON)}$ = 0V $I_{D(ON)}$ = ( ), $V_{GS(OFF)}$ = [ ]		25		50		100	ns
				25		40		80	
				(20) [-10]		(10) [-6]		(5) [-4]	(mA) [V]

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

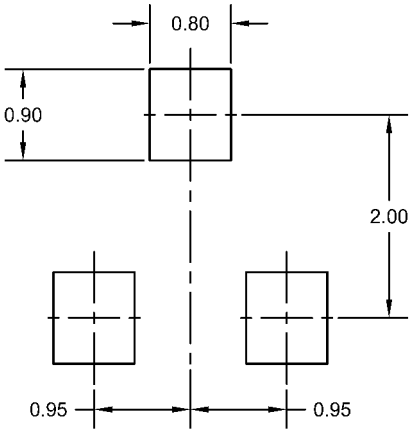






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

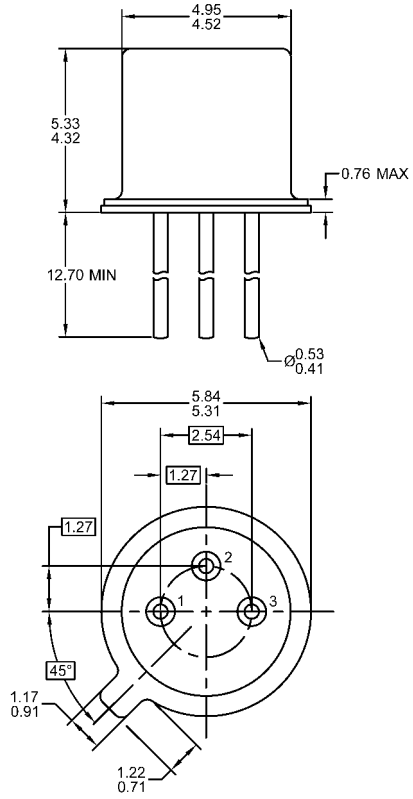
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

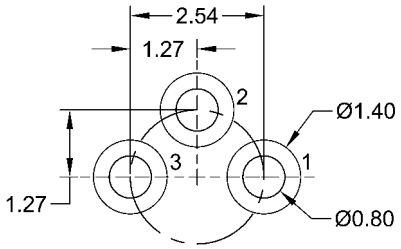
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

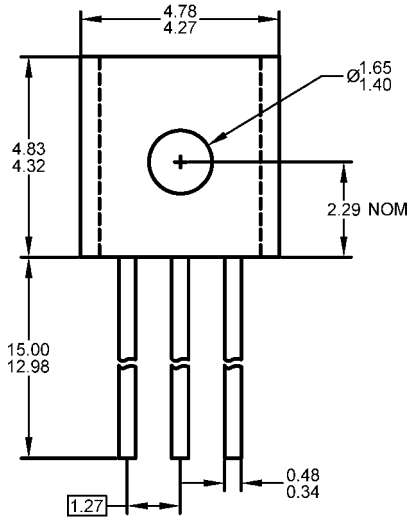
Suggested Through-Hole Layout

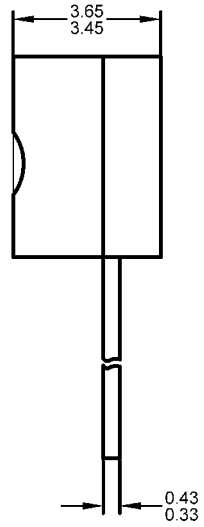


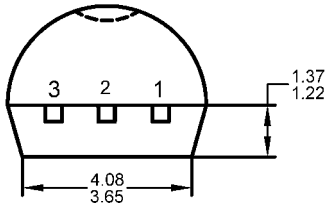
1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

TO-92 Mechanical and Layout Data

Package Outline Data

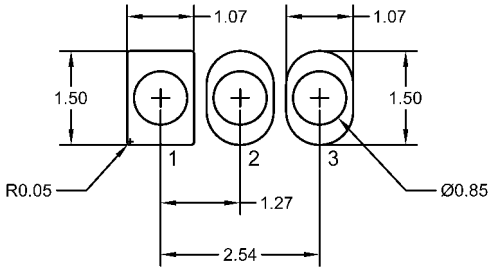






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.