IFN146 Dual Matched N-Channel JFET

Features

- InterFET N0450H Geometry
- Low Noise: 1.1 nV/√Hz Typical
- High Gain: 30mS Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

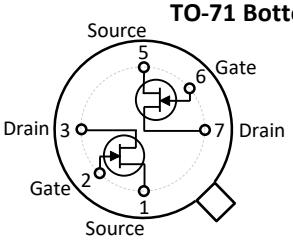
Applications

- Low-Noise Audio Amplifier
- Differential Amplifier
- Replacement for Japanese 2SK146

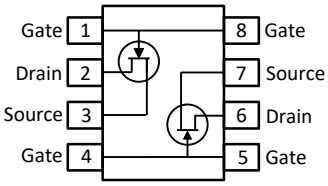
Description

The -50V InterFET IFN146 is a low noise high gain replacement for the Japanese 2SK146 JFET. Gate leakages are typically less than 50pA at room temperatures. The TO-71 package is hermetically sealed and suitable for military applications.

TO-71 Bottom View



SOIC8 Top View



Product Summary

Parameters		IFN146 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-40	V
I_{DSS}	Drain to Source Saturation Current	30 (max)	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.3	V
G_{FS}	Forward Transconductance	20	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN146	Through-Hole	TO-71	Bulk
SMP146	Surface Mount	SOIC8	Bulk
SMP146TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFN146COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFN146CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	10	mA
P_D	Continuous Device Power Dissipation	375	mW
P	Power Derating	3	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

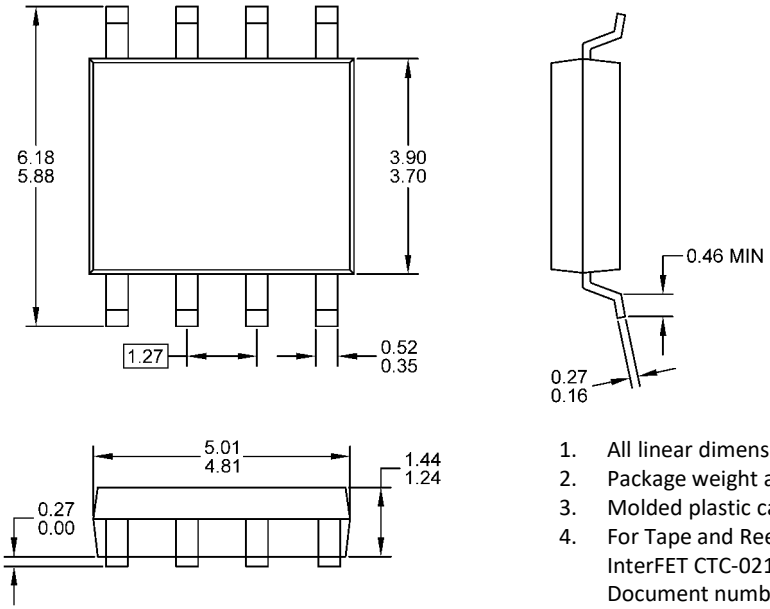
Parameters		Conditions	IFN146		Unit
			Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-40		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -30V, V_{DS} = 0V, T_A = 25°C V_{GS} = -30V, V_{DS} = 0V, T_A = 150°C		-1 -1	nA µA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 1µA	-0.3	-1.2	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 10V (Pulsed)		30	mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	IFN146			Unit
			Min	Typ	Max	
G_{FS}	Forward Transconductance	V_{DS} = 10V, V_{GS} = 0V, I_{DSS} = 5mA, f = 1kHz	20	30		mS
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz			75	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 10V, I_D = 0A, f = 1kHz			15	pF
NF	Noise Figure	V_{DS} = 10V, I_D = 5mA, R_G = 100Ω, f = 1kHz		1		dB
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 10V, I_D = 5mA			20	mV

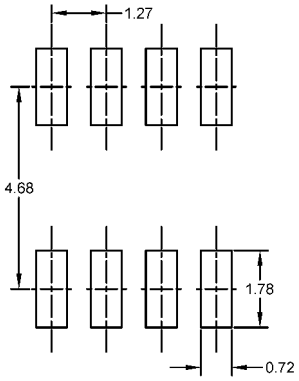
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

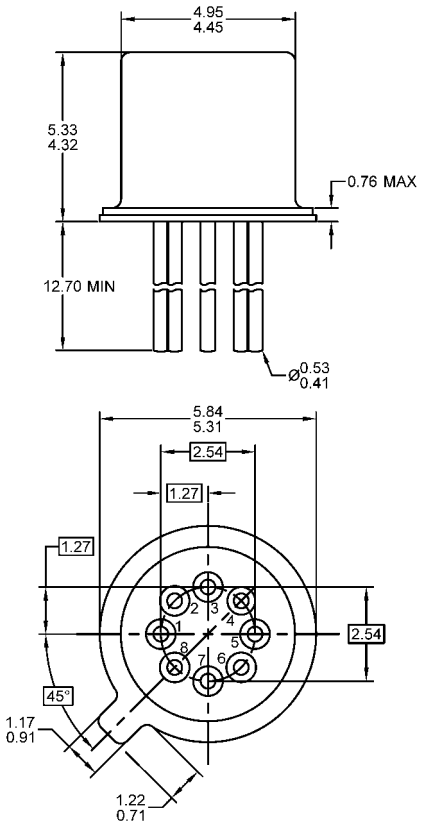
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

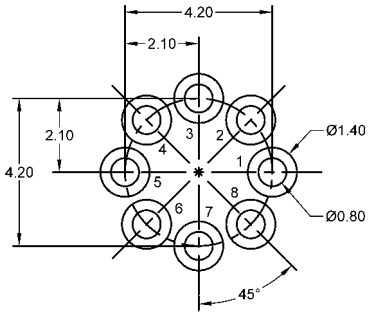
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.