

IFN3957, IFN3958 Dual Matched N-Channel JFET

Features

- InterFET [N0016H Geometry](#)
- Low gate leakage: 750fA typical @20V
- Low Ciss: 3pF typical
- Typical gain: 2mS
- Typical cutoff voltage: -2.5V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: [InterFET SPICE](#)

Industry Standard Crosses

- TBD

InterFET Similar Parts

- 2N4220-1A, 2N4340-1, 2N4867-8-9A
- IFN105, IFN40
- J201-2, J203-4
- VCR4N

InterFET Dual Parts

- IFNU401-2-3, IFNU404-5-6, IFN5197-8-9

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

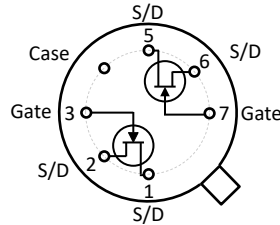
The -50V InterFET IFN3957 and IFN3958 matched pair JFET's are targeted for high input impedance applications for mid to high frequency designs. Gate leakages are typically 10pA at room temperatures. Parts are matched down to 5mV. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

Ordering Information

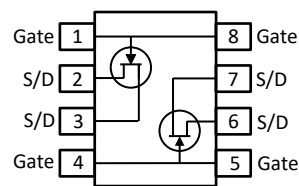
Part Number	Description	Case	Packaging
IFN3957; IFN3958	Through-Hole	TO-71	Bulk
SMP3957; SMP3958	Surface Mount	SOIC8	Bulk
SMP3957TR; SMP3958TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFN3957COT; IFN3958COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFN3957CFT; IFN3958CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

TO-71 Bottom View



SOIC8 Top View



NOTE: S/D pins are interchangeable Source Drain connections



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	TO-71	SOIC-8	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-20	-20	V
I_{FG} Continuous Forward Gate Current	50	50	mA
P_{D} Continuous Device Power Dissipation ¹	500	350	mW
P Power Derating ¹	3.3	2.8	mW/ $^\circ\text{C}$
T_{J} Operating Junction Temperature	-65 to 175	-55 to 150	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 175	-55 to 150	$^\circ\text{C}$

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IFN3957, IFN3958			Unit
		Min	Typ	Max	
$V_{(\text{BR})\text{GSS}}$ Gate to Source Breakdown Voltage	$I_{\text{G}} = -1\mu\text{A}, V_{\text{DS}} = 0\text{V}$	-50			V
I_{GSS} Gate to Source Reverse Current	$V_{\text{GS}} = -30\text{V}, V_{\text{DS}} = 0\text{V}, T_A = 25^\circ\text{C}$			-100	pA
	$V_{\text{GS}} = -30\text{V}, V_{\text{DS}} = 0\text{V}, T_A = 125^\circ\text{C}$			-500	nA
I_{G} Gate Operating Current	$V_{\text{DS}} = 20\text{V}, I_{\text{D}} = 200\mu\text{A}, T_A = 25^\circ\text{C}$			-50	pA
	$V_{\text{DS}} = 20\text{V}, I_{\text{D}} = 200\mu\text{A}, T_A = 125^\circ\text{C}$			-250	nA
$V_{\text{GS}(\text{OFF})}$ Gate to Source Cutoff Voltage	$V_{\text{DS}} = -20\text{V}, I_{\text{G}} = 1\text{nA}$	-1		-4.5	V
V_{GS} Gate Source Voltage	$V_{\text{DS}} = 20\text{V}, I_{\text{D}} = 50\mu\text{A}$			-4.2	V
	$V_{\text{DS}} = 20\text{V}, I_{\text{D}} = 200\mu\text{A}$	-0.5		-4	
$V_{\text{GS}(\text{F})}$ Gate Source Forward Voltage	$V_{\text{DS}} = 0\text{V}, I_{\text{G}} = 1\text{mA}$			2	
I_{DSS} Drain to Source Saturation Current	$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}$ (Pulsed)	0.5		5	mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

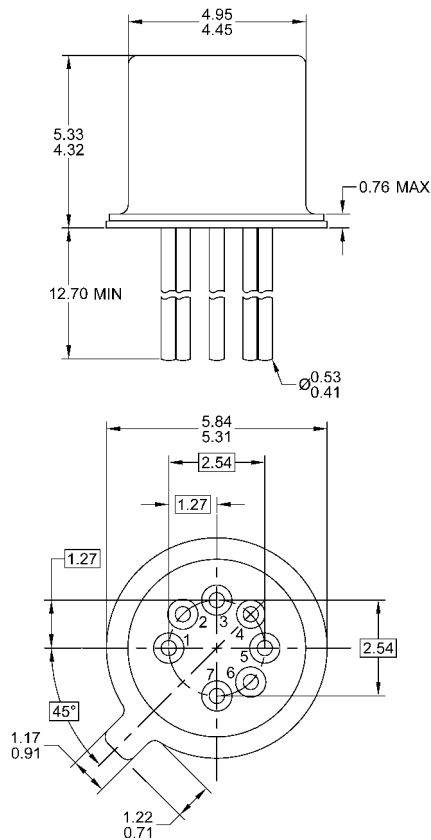
Parameters	Conditions	IFN3957, IFN3958			Unit
		Min	Typ	Max	
G_{FS} Forward Transconductance	$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{kHz}$ $V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}, f = 200\text{MHz}$	1000 1000		3000	μS
G_{OS} Output Conductance	$V_{\text{DS}} = 20\text{V}, f = 1\text{kHz}$			35	μS
C_{iss} Input Capacitance	$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$			4	pF
C_{rss} Reverse Capacitance	$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$			1.2	pF
NF Noise Figure	$V_{\text{DS}} = 20\text{V}, f = 10\text{Hz}, R_{\text{G}} = 10\text{M}\Omega$			0.5	dB
$ I_{\text{G1}} - I_{\text{G2}} $ Differential Gate Current	$V_{\text{DS}} = 20\text{V}, I_{\text{D}} = 200\mu\text{A}, T_A = 125^\circ\text{C}$			10	nA
$I_{\text{DSS1}}/I_{\text{DSS2}}$ Saturation Drain Current Ratio	$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}$	IFN3957 0.90		1	
		IFN3958 0.85		1	
$ V_{\text{GS1}} - V_{\text{GS2}} $ Differential Gate Source Voltage	$V_{\text{DS}} = 20\text{V}, I_{\text{D}} = 200\mu\text{A}$	IFN3957		20	mV
		IFN3958		25	
$\frac{ V_{\text{GS1}} - V_{\text{GS2}} }{\Delta T}$ Differential Gate Source Voltage with Temperature	$V_{\text{DS}} = 20\text{V}, I_{\text{D}} = 200\mu\text{A}$ $T_0 = -55^\circ\text{C}$ to 125°C	IFN3957		5	mV/ $^\circ\text{C}$
		IFN3958		5	
$g_{\text{fs1}}/g_{\text{fs2}}$ Transconductance Ratio	$V_{\text{DS}} = 20\text{V}, I_{\text{D}} = 200\mu\text{A}, f = 1\text{kHz}$	IFN3957 0.90		1	
		IFN3958 0.85		1	





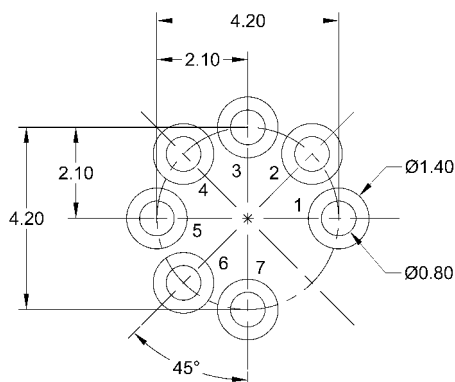
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

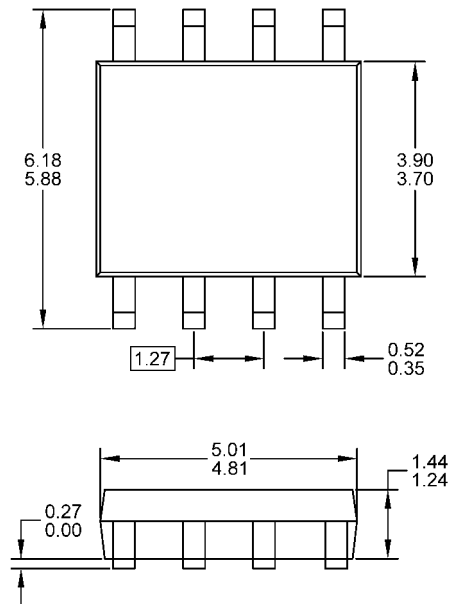
Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

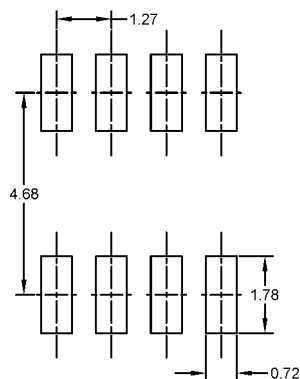
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit

www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 1	N/A	N/A
ESD	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM

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