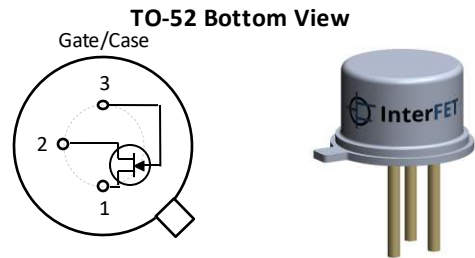


IFN5432, IFN5433, IFN5434 N-Channel JFET

Features

- InterFET [N0903L Geometry](#)
- Low Noise: 0.7 nV/VHz Typical
- High Gain: 200mS Typical
- Low $R_{ds(on)}$: 5 Ohms Max (IFN5432)
- RoHS Compliant
- SMT, TH, and Bare Die Package options.



Applications

NOTE: S/D pins are interchangeable Source Drain connections

- General: Amplifiers; Low leakage switches; Signal mixers
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Preamplifier speaker drive; Microphone impedance transformation and drive; Phono preamplifiers
- Military/Aero: Radar and communication systems; Missiles and guidance systems; Radiation detection
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment

Description

The -25V InterFET IFN5432, IFN5433, and IFN5434 are targeted for Low resistance switches and choppers. The TO-52 package is hermetically sealed and suitable for military applications.

Ordering Information

Part Number	Description	Case	Packaging
IFN5432; IFN5433; IFN5434	Through-Hole	TO-52	Bulk
IFN5432COT; IFN5433COT IFN5434COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFN5432CFT; IFN5433CFT IFN5434CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	TO-52	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG} Continuous Forward Gate Current	50	mA
P_D Continuous Device Power Dissipation ¹	420	mW
P Power Derating ¹	2.8	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-65 to 175	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 175	$^\circ\text{C}$

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

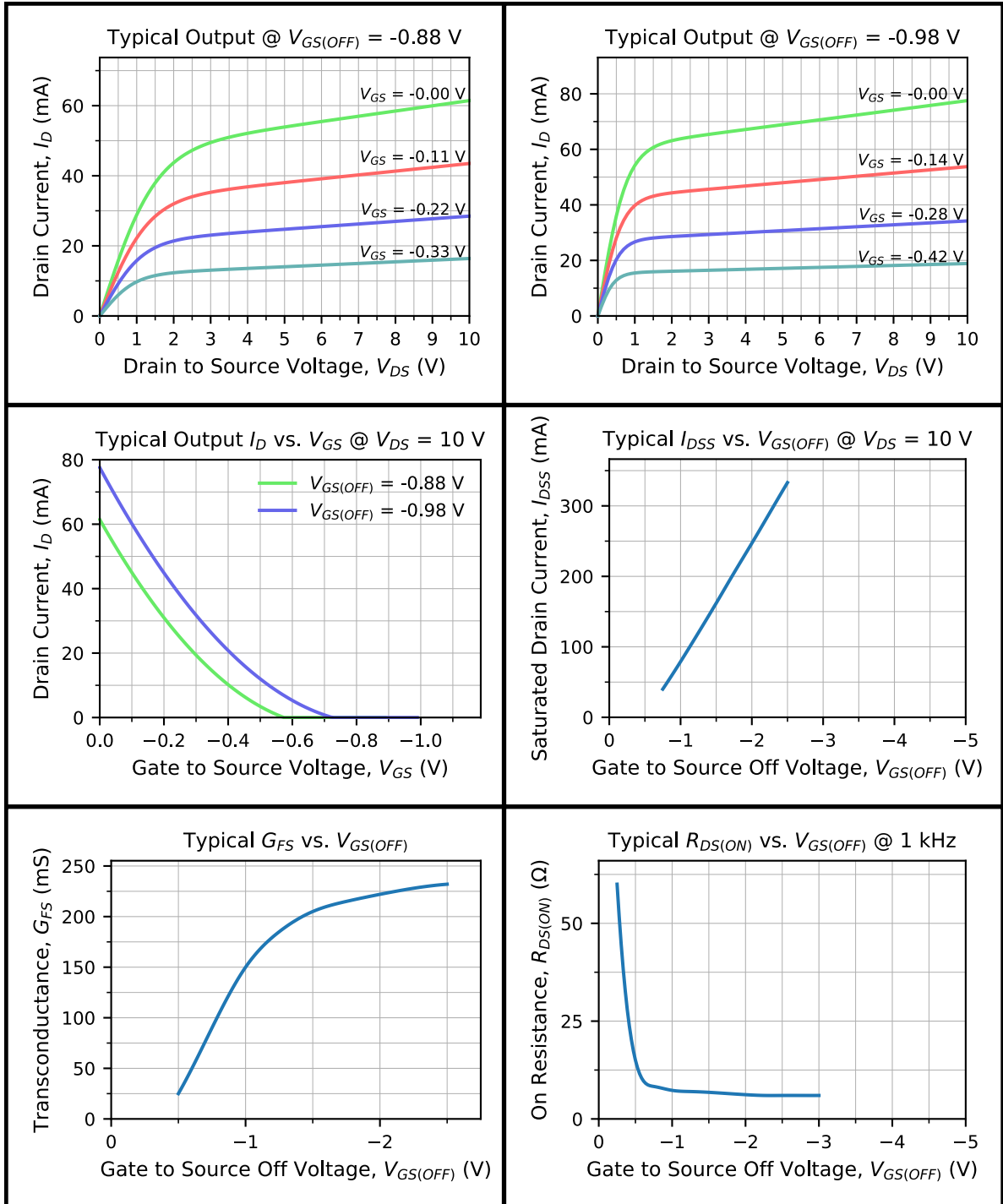
Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IFN5432		IFN5433		IFN5434		Unit
		Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu A$	-25		-25		-25		V
I_{GSS} Gate to Source Reverse Current	$V_{DS} = -15V, V_{GS} = 0V, T_A = 25^\circ\text{C}$		-200		-200		-200	pA
	$V_{DS} = -15V, V_{GS} = 0V, T_A = 150^\circ\text{C}$		-200		-200		-200	nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 5V, I_D = 3nA$	-4	-10	-3	-9	-1	-4	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 15V$ (Pulsed)	150		100		30		mA
$I_{D(OFF)}$ Drain Cutoff Current	$V_{DS} = 5V, V_{GS} = -10V, T_A = 25^\circ\text{C}$		200		200		200	pA
	$V_{DS} = 5V, V_{GS} = -10V, T_A = 150^\circ\text{C}$		200		200		200	nA
$V_{DS(ON)}$ Drain to Source ON Voltage	$V_{GS} = 0V, I_D = 10mA$		50		70		100	mV
$R_{DS(ON)}$ Static Drain to Source ON Resistance	$V_{GS} = 0V, I_D = 10mA$	2	5		7		10	Ω

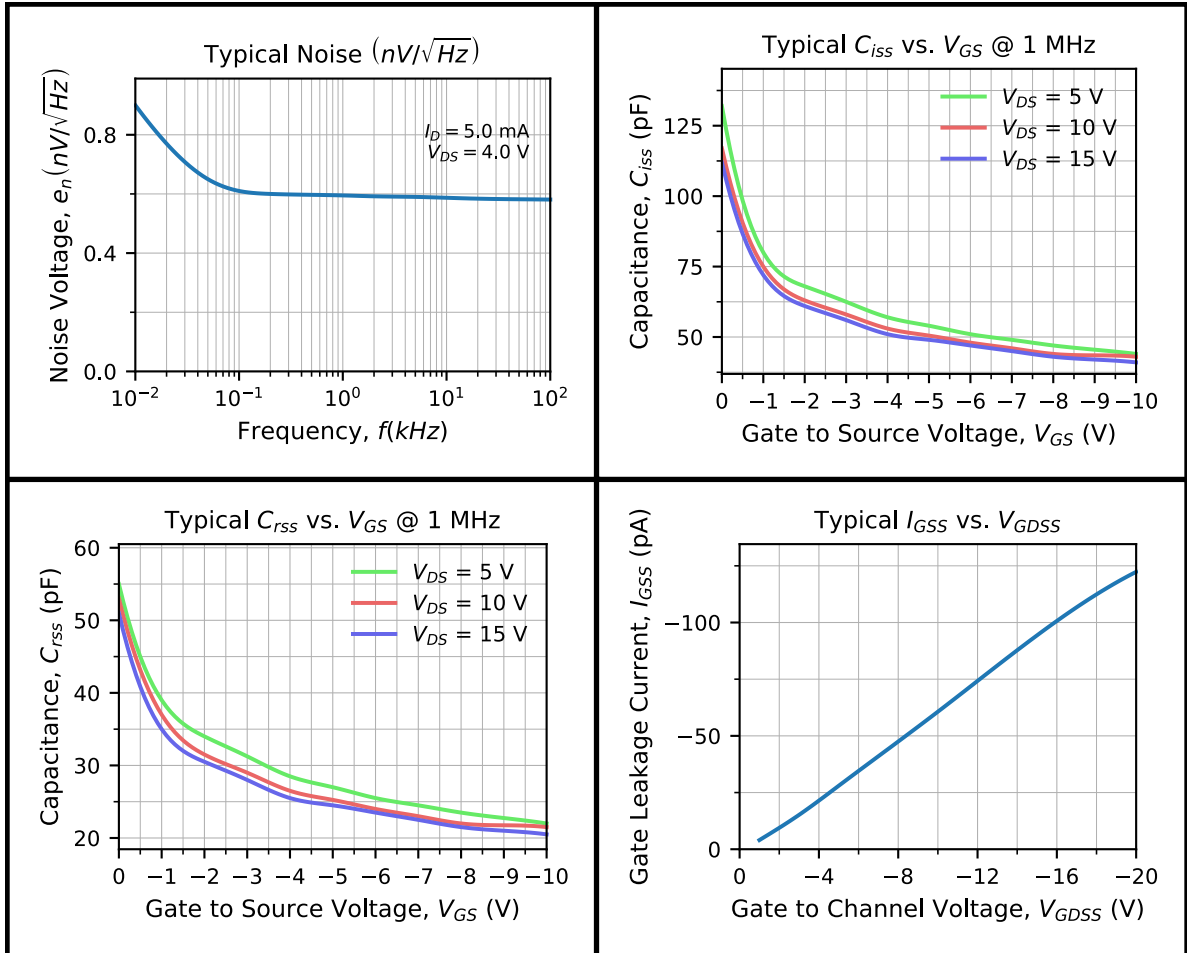
Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IFN5432		IFN5433		IFN5434		Unit
		Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$ Drain to Source ON Resistance	$V_{GS} = 0V, I_D = 0A, f = 1kHz$		5		7		10	Ω
C_{iss} Input Capacitance	$V_{DS} = 0V, V_{GS} = -10V, f = 1MHz$		60		60		60	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 0V, V_{GS} = -10V, f = 1MHz$		20		20		20	pF
$t_{d(ON)}$ Turn-On Delay Time	$V_{DD} = 1.5V, V_{GS(ON)} = 0V,$ $V_{GS(OFF)} = -12V, I_{D(ON)} = 10mA$		4		4		4	ns
t_r Rise Time			1		1		1	ns
$t_{d(OFF)}$ Turn-Off Delay Time			6		6		6	ns
t_f Fall Time			30		30		30	ns

Typical IFN5432, IFN5433, INF5434 Characteristics

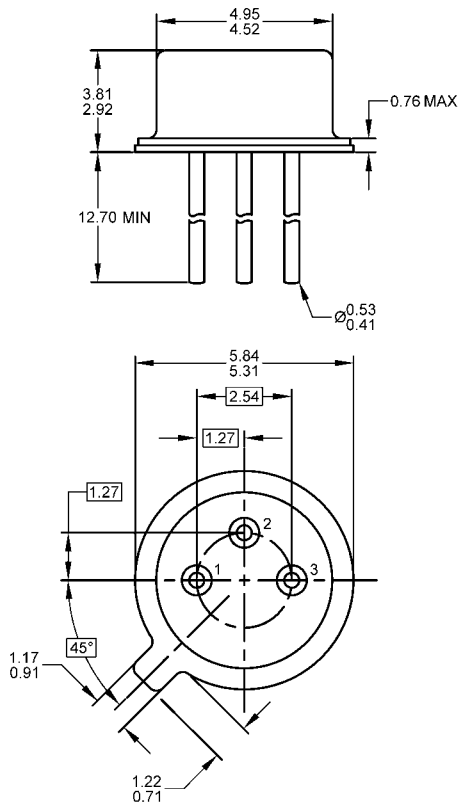


Typical IFN5432, IFN5433, INF5434 Characteristics (Continued)



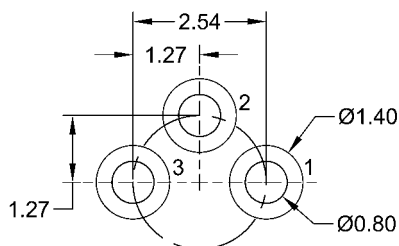
TO-52 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.26 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 2	N/A	N/A
ESD	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM

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