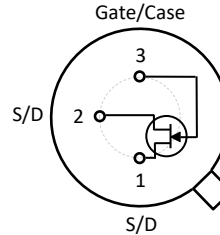


IFNU310 N-Channel JFET

Features

- InterFET [N0072S Geometry](#)
- Low gate leakage: 750fA typical @10V
- Low Ciss: 3pF typical
- Typical noise: 2.0 nV/VHz
- Typical gain: 2mS
- Typical cutoff voltage: -2.5V
- Typical I_{DSS}: 12mA
- Typical BV_{GSS}: -35V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: [InterFET SPICE](#)

TO-52 Bottom View



NOTE: S/D pins are interchangeable Source Drain connections

Industry Standard Crosses

- TBD

InterFET Similar Parts

- U310

InterFET Dual Parts

- U431

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Pre-Amps
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The -25V InterFET IFNU310 JFET is targeted for higher gain VHF amplifiers, mixers, and oscillators. Gate leakages are typically less than 10pA at room temperatures.



Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFNU310	Through-Hole	TO-52	Bulk



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG} Continuous Forward Gate Current	50	mA
P_D Continuous Device Power Dissipation ¹	500	mW
P Power Derating ¹	3.3	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-65 to 175	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 175	$^\circ\text{C}$

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

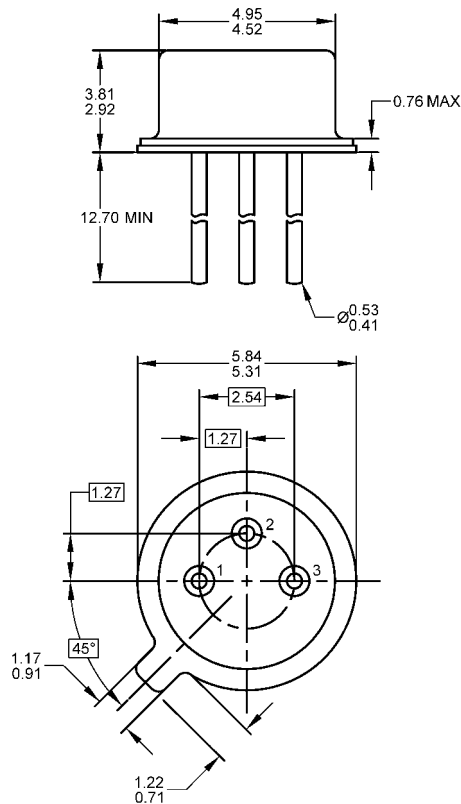
Parameters	Conditions	IFNU310			Unit
		Min	Typ	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu A$	-25			V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -15V, V_{DS} = 0V, T_A = 25^\circ\text{C}$ $V_{GS} = -15V, V_{DS} = 0V, T_A = 125^\circ\text{C}$			-150 -150	pA nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10V, I_D = 1nA$	-2.5		-6	V
$V_{GS(F)}$ Gate to Source Forward Voltage	$V_{DS} = 0V, I_G = 10mA$			1	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 10V$ (Pulsed)	24		60	mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IFNU310			Unit
		Min	Typ	Max	
G_{FS} Forward Transconductance	$V_{DS} = 10V, I_D = 10mA, f = 1kHz$	10	17		mS
	$V_{DS} = 10V, I_D = 10mA, f = 105MHz$		15		
	$V_{DS} = 10V, I_D = 10mA, f = 450MHz$		14		
G_{OS} Output Conductance	$V_{DS} = 10V, I_D = 10mA, f = 1kHz$			250	μS
	$V_{DS} = 10V, I_D = 10mA, f = 105MHz$		0.18		
	$V_{DS} = 10V, I_D = 10mA, f = 450MHz$		0.32		
C_{dg} Drain Gate Capacitance	$V_{DS} = 10V, V_{GS} = -10V, f = 1MHz$			2.5	pF
C_{gs} Source Gate Capacitance	$V_{DS} = 10V, V_{GS} = -10V, f = 1MHz$			5	pF
e_n Noise Voltage	$V_{DS} = 10V, I_D = 10mA, f = 100kHz$		10		nV/ $\sqrt{Hz}$
NF Noise Figure	$V_{DS} = 10V, I_D = 10mA, f = 105MHz$		1.5	2	dB
	$V_{DS} = 10V, I_D = 10mA, f = 450MHz$		2.7	3.5	

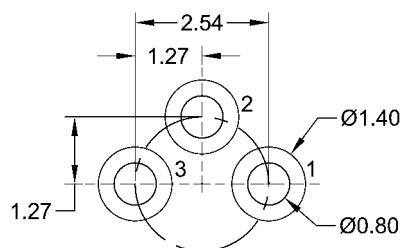
TO-52 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.26 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit

www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 2	N/A	N/A
ESD	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM

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