J110, J110A N-Channel JFET

Features

- InterFET N0450S Geometry
- Low Noise: 1 nV/√Hz Typical
- High Gain: 100mS Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

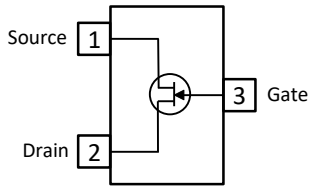
Applications

- Choppers
- Commutators
- Analog Switches

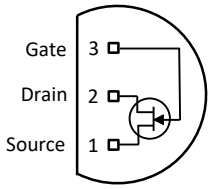
Description

The -25V InterFET J110 and J110A JFET's are targeted for high gain low noise switching, commutator, and chopper applications.

SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters		J110 Min	J110A Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-25	-25	V
I_{DSS}	Drain to Source Saturation Current	10	10	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.5	-0.5	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J110; J110A	Through-Hole	TO-92	Bulk
SMPJ110; SMPJ110A	Surface Mount	SOT23	Bulk
SMPJ110TR; SMPJ110ATR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
J110COT; J110ACOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
J110CFT; J110ACFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-25	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	360	mW
P	Power Derating	3.27	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

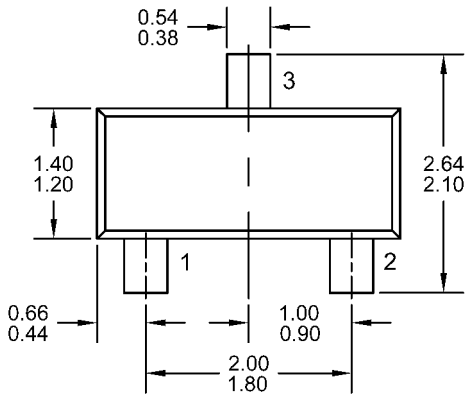
Parameters		Conditions	J110		J110A		Unit
			Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-25		-25		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -15V, V_{DS} = 0V		-3		-3	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 5V, I_D = 1µA	-0.5	-4	-0.5	-4	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 15V (Pulsed)	10		10		mA
I_D	Drain Cutoff Current	V_{DS} = 5V, V_{GS} = -10V		3		3	nA

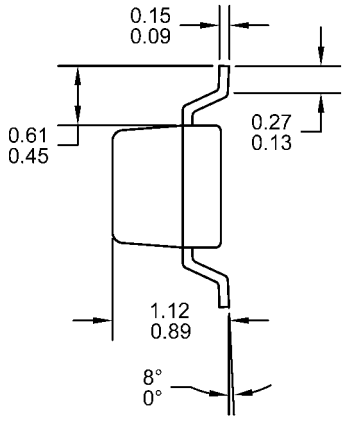
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

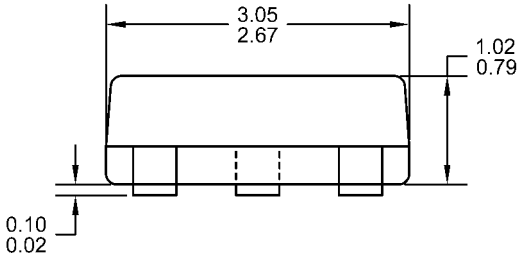
Parameters		Conditions	J110		J110A		Unit
			Min	Max	Min	Max	
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{DS} <= 0.1V, V_{GS} = 0V, f = 1kHz		18		25	Ω
C_{gd}	Drain Gate Capacitance	V_{DS} = 0V, V_{GS} = -10V, f = 1MHz		15		15	pF
C_{gs}	Input Capacitance	V_{DS} = 0V, V_{GS} = -10V, f = 1MHz		15		15	pF
$C_{gd} + C_{gs}$	Drain + Source Gate Capacitance	V_{DS} = V_{GS} = 0V, f = 1MHz		85		85	pF
$t_{d(ON)}$	Turn ON Delay Time	V_{DD} = 1.5V, $V_{GS(OFF)}$ = -5V, R_L = 150 Ω	4 (typ)		4 (typ)		ns
t_r	Rise Time		1 (typ)		1 (typ)		ns
$t_{d(OFF)}$	Turn OFF Delay Time		6 (typ)		6 (typ)		ns
t_f	Fall Time		30 (typ)		30 (typ)		ns

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

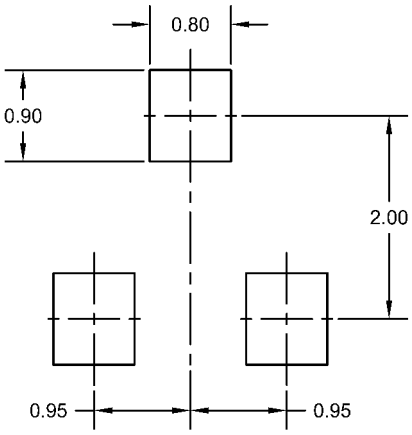






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

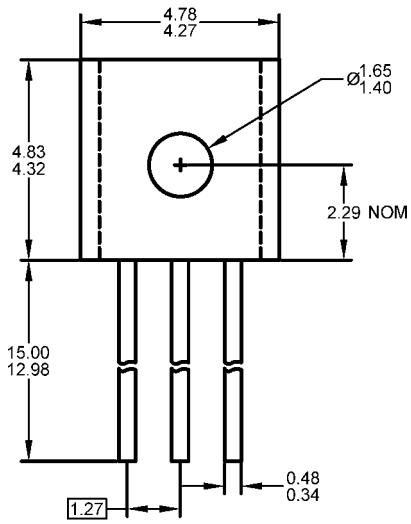
Suggested Pad Layout

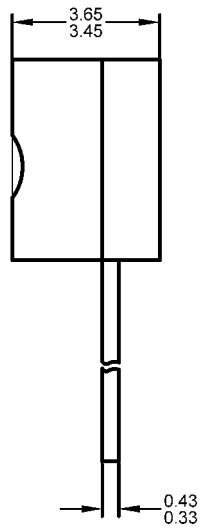


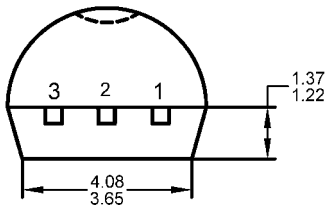
1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

TO-92 Mechanical and Layout Data

Package Outline Data

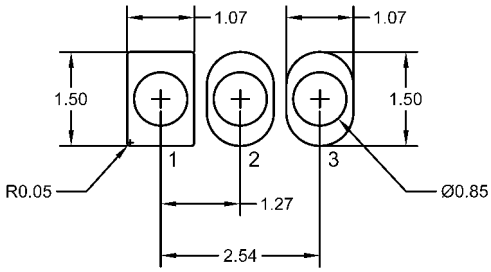






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.