J500, J501, J502 Current Regulator Diode

Features

- InterFET N0016H Geometry
- Low Noise: 5 nV/√Hz Typical
- Low Capacitance: 2pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

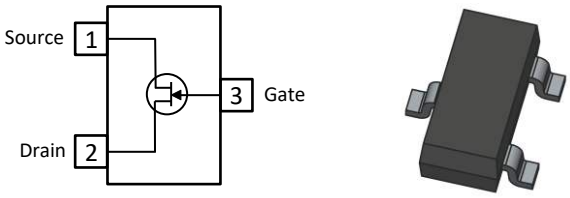
Applications

- Current Regulation
- Current Limiting

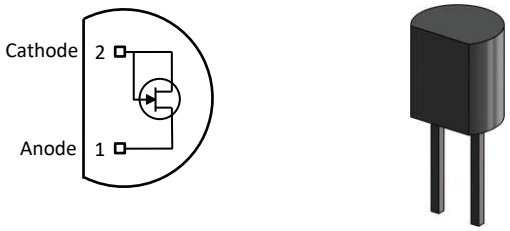
Description

The 50V InterFET J500, J501, and J502 JFET's are targeted for current regulation and limiting applications. The SOT23 package is pinned out as a standard JFET and is required by the user to connect the Gate to the Source or Drain.

SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters		J500 Min	J501 Min	J502 Min	Unit
V_{OP}	Peak Operating Voltage	50 (typ)	50 (typ)	50 (typ)	V
I_{F1}	Forward Current	0.192	0.264	0.344	mA
V_L	Limiting Voltage	0.8 (typ)	0.9 (typ)	1.1 (typ)	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J500; J501; J502	Through-Hole	TO-92-2L	Bulk
SMPJ500; SMPJ501; SMPJ502	Surface Mount	SOT23	Bulk
SMPJ500TR; SMPJ501TR; SMPJ502TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
J500COT; J501COT; J502COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
J500CFT; J501CFT; J502CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{OP}	Peak Operating Voltage	50	V
I_{FG}	Continuous Forward Gate Current	20	mA
P_D	Continuous Device Power Dissipation	360	mW
P	Power Derating	3.27	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

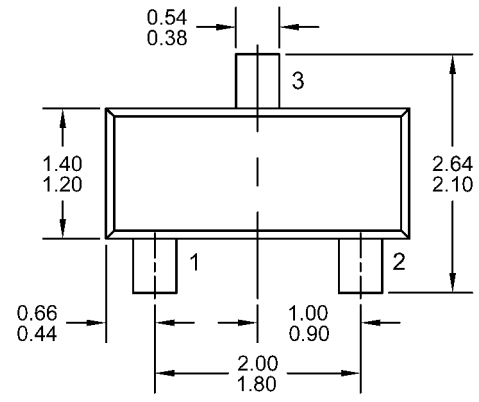
Parameters		Conditions	J500			J501			J502			Unit
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
I_{F1}	Forward Current	V_F = 25V	0.192	0.240	0.288	0.264	0.33	0.396	0.344	0.43	0.516	mA
V_L	Limiting Voltage	$I_F = 0.9\ I_{F(MIN)}$		0.8 (typ)	1.2 (typ)		0.9 (typ)	1.3 (typ)		1.1 (typ)	1.5 (typ)	V
V_{OP}	Peak Operating Voltage	$I_F = 1.1\ I_{F(MAX)}$	50			50			50			V

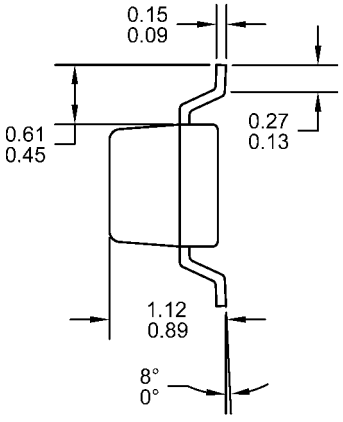
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

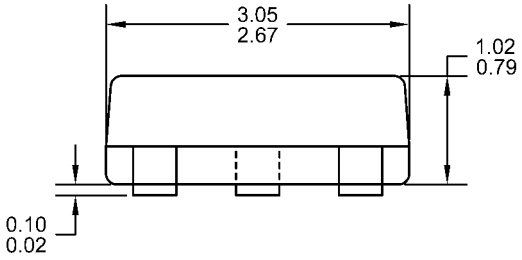
Parameters		Conditions	J500			J501			J502			Unit
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Z_{fi}	Dynamic Impedance	V_F = 25V, f = 1kHz	4	8		2.2	6		1.5	4.4		MΩ
C_F	Anode-Cathode Capacitance	V_F = 25V, f = 1kHz		2			2			2		pF

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

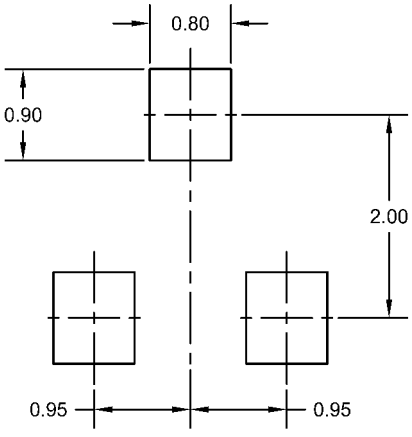






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

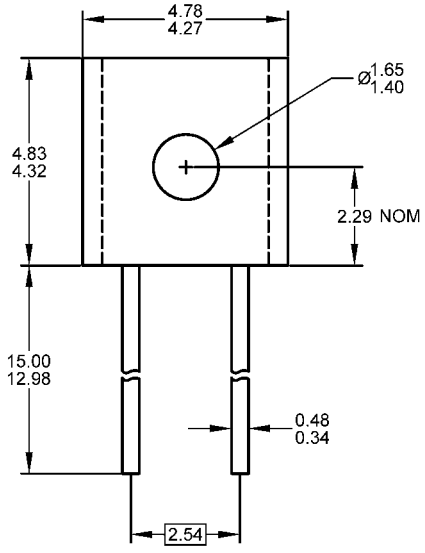
Suggested Pad Layout

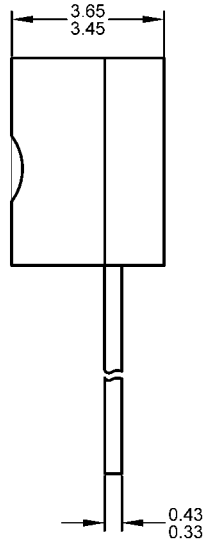


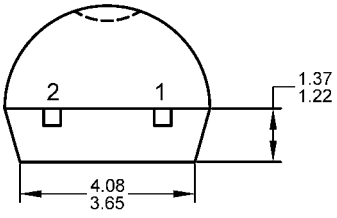
1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

TO-92-2L Mechanical and Layout Data

Package Outline Data

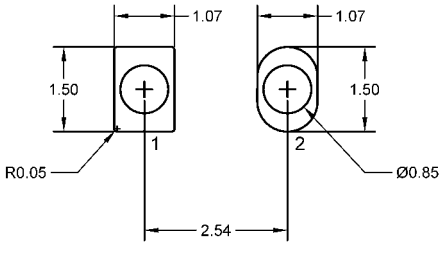






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.